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AT&S HDI Technology

Desinrules and Cost Optimization

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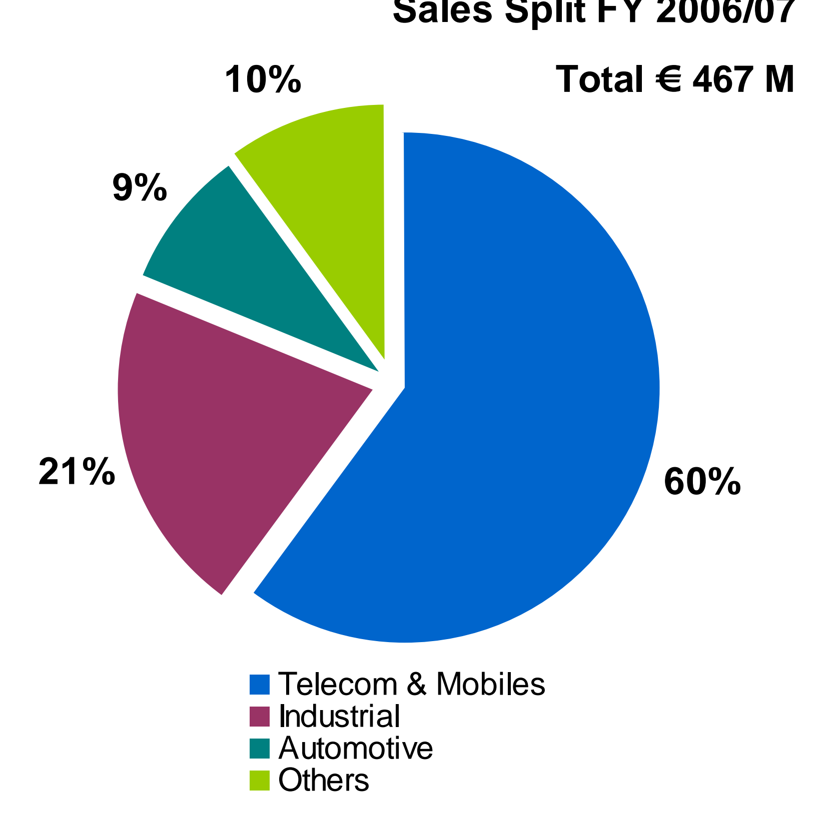
AT&S At A Glance

- Founded in 1982, publicly traded since 1999
- Europe‘s largest supplier of printed wiring boards (PWB)
- India’s largest supplier of standard PWBs
- One of world’s top producers of HDI PWBs (for mobile phones)
- 6000 employees in Austria, China, India and Korea

AT&S' Major Business Segments

- **Telecom & Mobiles**
  - Handheld devices
  - Network components
- **Industrial**
  - Industrial applications
  - Medical devices
  - White goods
  - Defense industry
- **Automotive**
  - Automobile components
- **Others**
  - Design, Assembly and Foundry Services



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HQ, Vienna-Austria: 60 People

Shanghai I+II - China: 2.800 People

Leoben-Austria: 1.500 People

Ansan-S.Korea: 300 People

Fehring-Austria: 450 People

Klagenfurt-Austria: 200 People

Nanjangud-India: 700 People

AT&S

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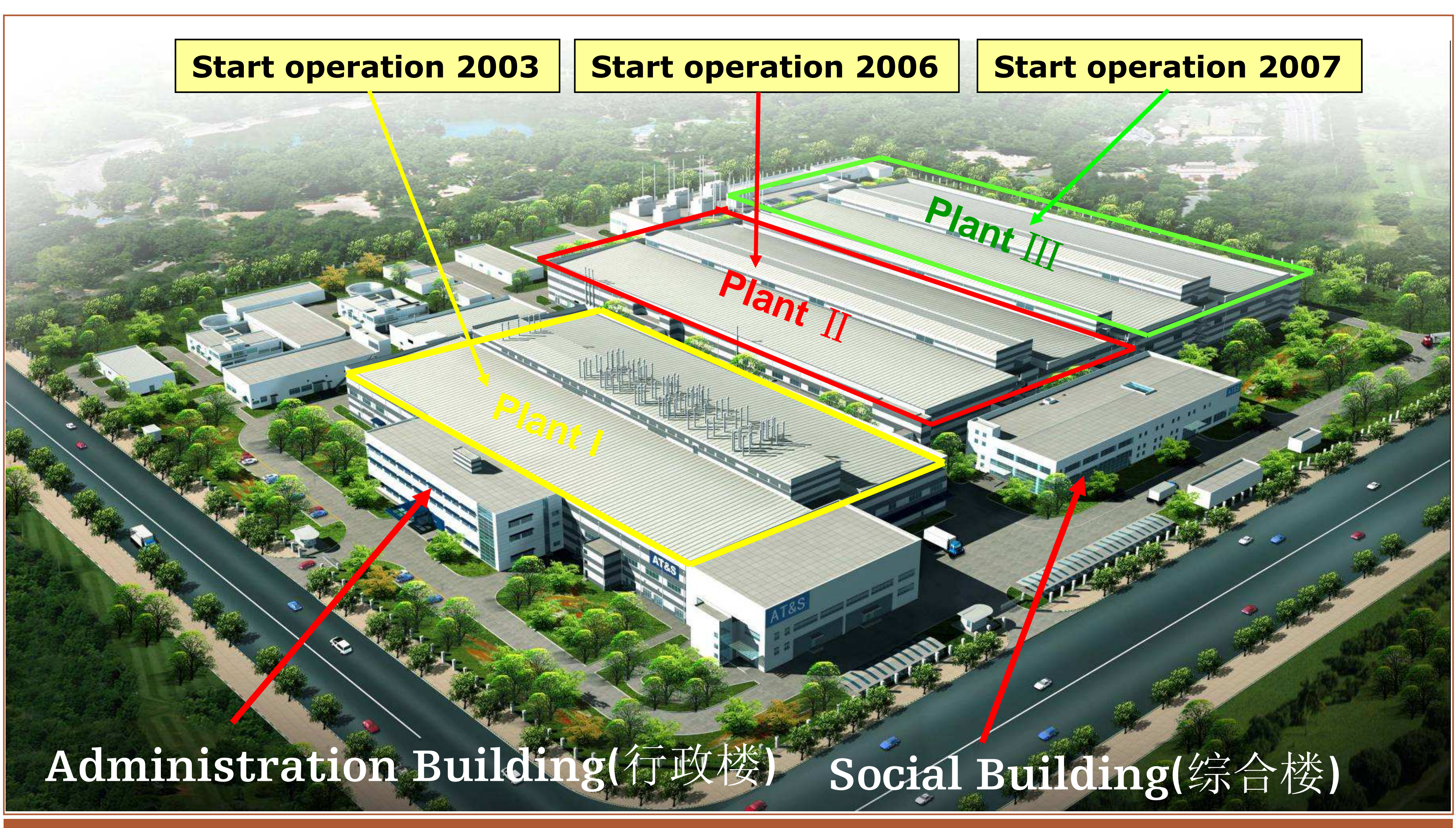

HDI Standard Design Rules

HDI Advanced Design Rules

HDI Design (Multilayers with 4 µ-Via layer) 2-N-2 Construction:
Build up material.: RCF or 106 / 1080 Prepreg

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* ...60µm for max. 20 +/-10µm overall copper thickness

N=> 4ML / 6ML /8ML / 10ML /12ML/ 14ML

- HDI Standard Design Rules
- HDI Advanced Design Rules

HDI Design (Multilayers with 2 –N-2) Copper filled Via Construction: Design Values for RCC and 106 / 1037 Prepreg

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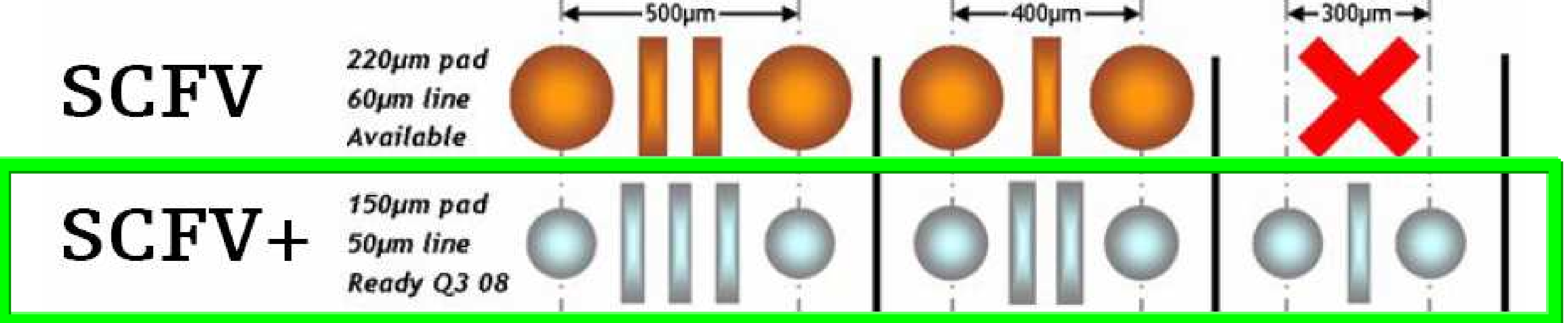
Next generation technology for redistribution of 400µm pitch BGA and below – SCFV+

- Cost-effective concept for ultra high density BGA redistribution
- 2 lines per channel capability at 400µm pitch BGA
- 1 line per channel at 300µm pitch
- Mass production ready, dependable reliability
- Ask for more details

	SCFV	SCFV+
BGA 400µm (pin amount)	~ 100	560
BGA Pad size (inner Layer)	220	150
µVia diameter	100	75
Dielectric	60µm	40µm
Registration (Laser pad – Laser hole)	+/- 60µm	+/- 37,5 µm
Line width & space	60µm	50µm
Solder mask registration	+/- 38µm	+/- 25µm



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SCFV 1	SCFV 2	SCFV 3
Staggered Micro-via; Composite; Buried via; Stacked Copper Filled Via	Composite; Buried via; Stacked Copper Filled Via	Stacked Copper Filled Via
Composite - 2 to 6 Layer	Composite - 2 to 6 Layer	All Layer Micro-via SCFV - internal layers Filled/not filled micro-via - external layer
Mechanical drilled Buried vias	Mechanical drilled Buried vias, plugged and plated	
Micro-vias staggered on Buried vias	Micro-via stacked on buried via	
SCFV - internal layers Filled/not filled micro-via - external layer	SCFV - internal layers Filled/not filled micro-via - external layer	

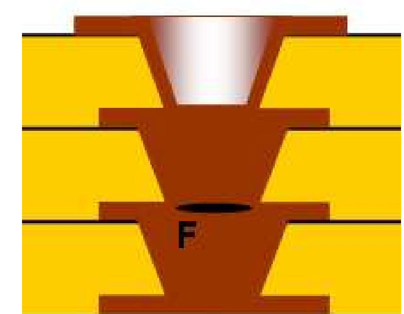
Increasing Interconnect Density →

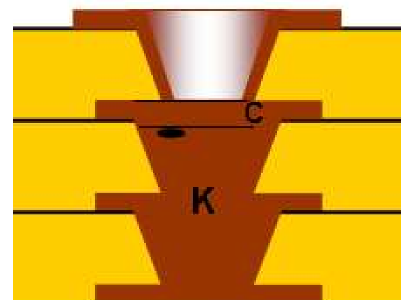
Specification

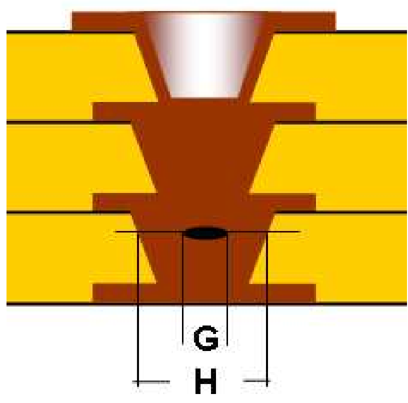
Topic	AT&S recommendation
Copper thickness at surface	12 - 22µm
Copper thickness in pth	min 10µm
Copper thickness in buried	min 10µm
Copper thickness in Laser	min 10µm or filled via
Breake out of µ-vias allowed as long space is same as min L/S	
Solder mask thickness at track < 60µm	min. 4µm
Solder mask thickness at edge of track	min. 4µm

Issue	Specification	
Raw material	Halogen free material (or Standard FR4)	
conductor width & space	Min 60µm (50µm for 0,4mm, 0,3mm BGA Area)	
Copper thickness at surface (each layer)	20µm +/-10µm (Due to Plating technology preferred)	
µvia connection at capture pad	100, (70µm for 40µm dielectric) diameter should be given in the Drill Table. The minimum diameter of the micro via (A) at capture pad is 50% of the nominal value.	A
Dimple	Max 15µm at inner layer Max 30µm at outer layer	
Plated through hole	Copper plating of plated through hole (pth) and copper filled µVias (SCFVias) at same time is possible but minimum distance between PTH and µ-Vias need to be evaluated.	

Issue	Specification
Void at capture pad	Delamination, void or resin impurities are not allowed on the vertical interface of two micro vias (F).
Void in copper filled µvia-hole	20% of the population of filled micro vias may have a small void in the micro via. The distance between void and the plated surface of the micro via should be more than the thickness of the copper pad (C). The maximum void width (G) shall be less than 25% of micro via diameter (H) measured at the point where the void is widest. The minimum copper between void and the outer edge of filled micro via (K) shall be min 10µm as in section.







Core / prep / RCC	CORE	CORE
Nominal thickness	80 – 100µm	60µm
Picture		
Drilling done by	Laser	Laser
Via – dia	150 µm	85 µm
Min. pad	280 µm	170 µm

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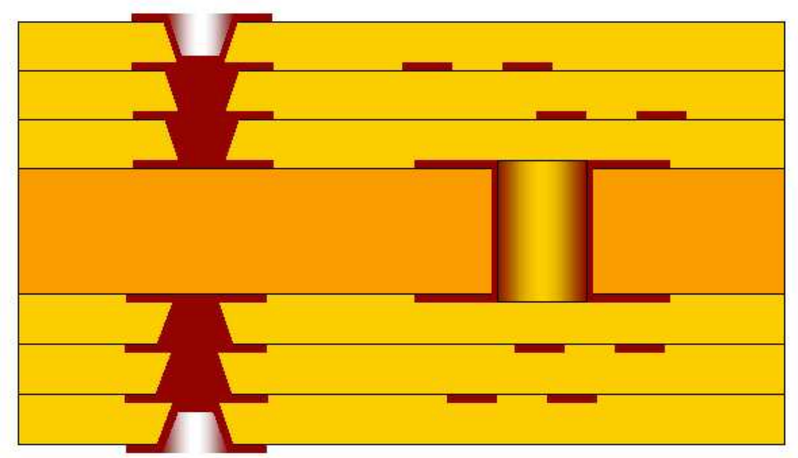
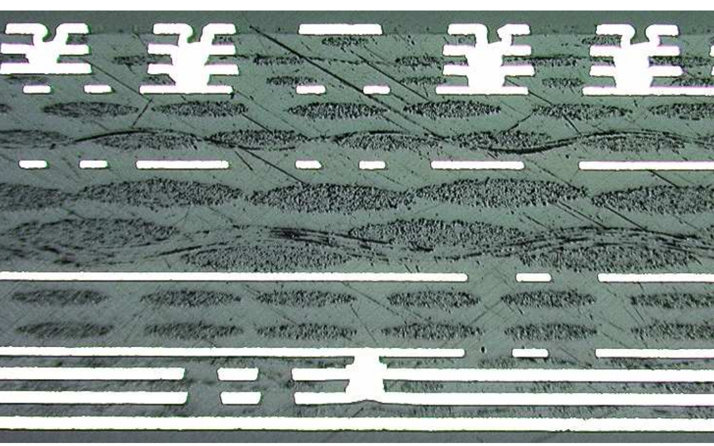
Prepreg / RCC	PREPREG	PREPREG	RCC
Nominal thickness	40, 50µm / 1037, 106prep	60µm / 1080prep	40µm
Picture			
Drilling done by	Laser	Laser	Laser
Via – dia	70, 100 µm	100 µm	70 µm
Min. pad	220 µm (150µm)	250 µm (220µm)	220µm (150µm)

HDI PCB 1-1-1-2-1-1-1 µ-Via Stacked





Stacked copper filled microvias

- ✓ Design density will increase
- ✓ Layer count reduction possible
- ✓ High reliable stacked microvias
- ✓ Alternative to conductive paste
- ✓ Qualification with halogenfree m.

Prepreg; RCC

Laminate

Prepreg; RCC

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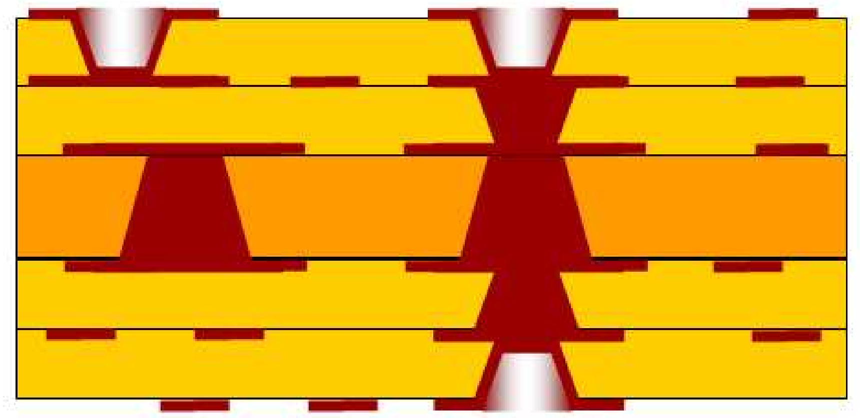
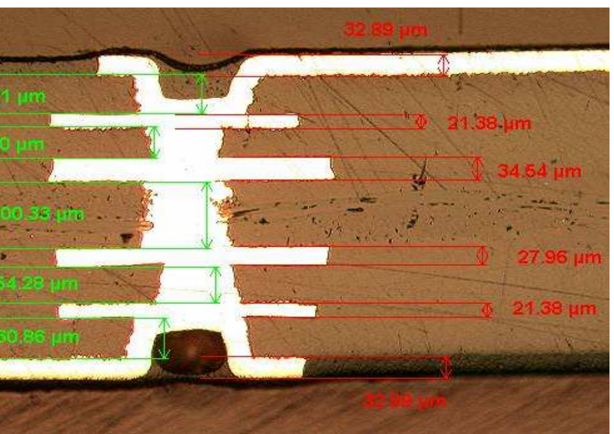
Stacked copper filled microvias (all layer)

HDI PCB 1-1-2-1-1 SCFV





Schematic HDI PCB Build – up AT&S Advanced

HDI PCB 1-1-4-1-1 µ-Via Stacked

HDI PCB 1-1-1-2-1-1-1 µ-Via Stacked

HDI PCB 1-1-1-4-1-1-1 µ-Via Stacked

HDI PCB 1-2-1 Stacked

HDI PCB 1-1-1-2-1-1-1 µ-Via Stacked

HDI PCB 1-1-1-2-1-1-1 SCFV

HDI PCB 1-1-2-1-1 SCFV

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Cost Optimization for Micro Via PCBs

Design, Processes, Materials, New Technologies

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HDI Cost optimization – Micro Via

HDI Cost optimization – Base Materials

HDI Cost optimization – Laser dielectric

HDI Cost optimization – Copper thickness

HDI Cost optimization – Utilization Vendor panel

HDI Cost optimization – Design

Cost impacts on printed circuit boards:

- **Build up** (1-N-1 / 2-N-2 / 3-N-3......)
- **Total Thickness** (Aspect Ratio)
- **Build up Materials** (RCC / FR4 / woven glass...)
- **Base Material** (TG / HF / Low CTE....)
- **Copper specification for Micro Vias / Plated through holes**
- **Size of pcb / panel** (Vendor production panel)
- **Design** (Track width / - spacing / Laser pads / PTH-Pads / annular ring.......)

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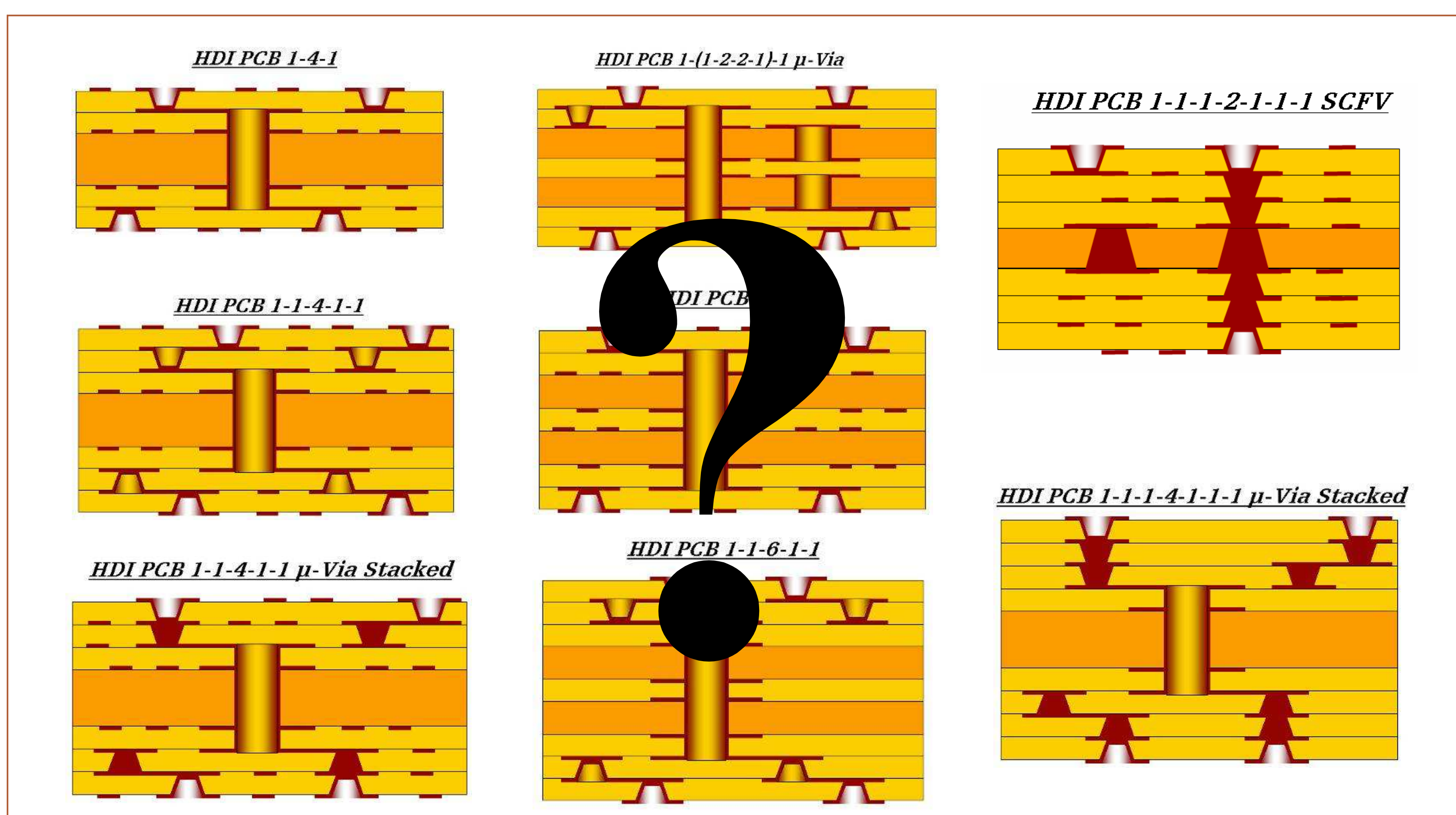

Cost comparison Micro Via Build ups

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160,00%
140,00%
120,00%
100,00%
80,00%
60,00%
40,00%
20,00%
0,00%

85,38%
100,00%
120,77%
136,92%
126,15%
114,08%

Aufbau 1-4-1
Aufbau 1-6-1
Aufbau 2-4-2
Aufbau 2-4-2 Filled Via
Aufbau 2-4-2 1,6 mm
Aufbau 2-4-2 0,8 mm

HDI PCB 1-4-1
HDI PCB 1-6-1
HDI PCB 1-1-4-1-1
HDI PCB 1-1-4-1-1 μ-Via Stacked
HDI PCB 1-1-4-1-1
HDI PCB 1-1-4-1-1

- HDI Cost optimization – Micro Via
- **HDI Cost optimization – Base Materials**
- HDI Cost optimization – Laser dielectric
- HDI Cost optimization – Copper thickness
- HDI Cost optimization – Utilization Vendor panel
- HDI Cost optimization – Design

Cost Comparison Base Material

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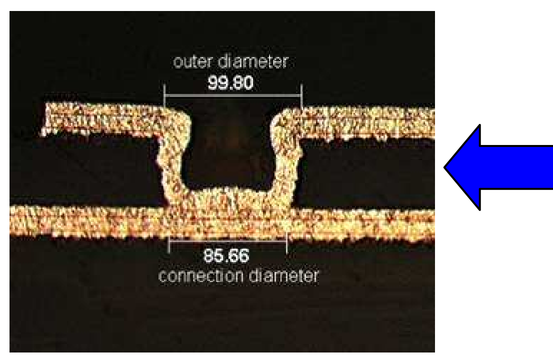
- HDI Cost optimization – Micro Via
- HDI Cost optimization – Base Materials
- **HDI Cost optimization – Laser dielectric**
- HDI Cost optimization – Copper thickness
- HDI Cost optimization – Utilization Vendor panel
- HDI Cost optimization – Design

Base Material for Laser (micro via) Dielectrics:

Optimum Aspect Ratio 1:1.4

(Dielectric : Laser diameter)



Type	Glass yarn	thickness µm*	µ-Via Ø
FR4	1037	40	50 -75
FR4	0106	45	80 - 100
FR4	1080	65	90 - 110
FR4	2 x 0106	100	130 - 150
FR4	2116	110	130 - 150
RCC	----	30	50 -75
RCC	----	50	80 -100
RCC	----	60	90-110

* nominal value without consideration of press and design tolerance

Cost Comparison Laser Dielectrics

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400,00%
350,00%
300,00%
250,00%
200,00%
150,00%
100,00%
50,00%
0,00%

210,23%
358,91%
153,80%
100%
307,59%
109,24%

RCC 50µm
1037
106
1080
2 x 0106
2116

- HDI Cost optimization – Micro Via
- HDI Cost optimization – Base Materials
- HDI Cost optimization – Laser dielectric
- **HDI Cost optimization – Copper thickness**
- HDI Cost optimization – Utilization Vendor panel
- HDI Cost optimization – Design

Cost comparison Copper thickness in PTH

HDI PCB 1-1-4-1-1

110,00%
105,00%
100,00%
95,00%
90,00%

97,01%
100,00%
102,55%

min. 15µm
min. 20µm
min. 25 µm

HDI Cost optimization – Micro Via

HDI Cost optimization – Base Materials

HDI Cost optimization – Laser dielectric

HDI Cost optimization – Copper thickness

HDI Cost optimization – Utilization Vendor panel

HDI Cost optimization – Design

Example .: PCB 160mm x 110 mm / 2-4-2 HDI Aufbau

Utilization 81 %

Cost 100 %

Increase of width by 2mm:

Utilization 66 %

Cost 122 %

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- HDI Cost optimization – Micro Via
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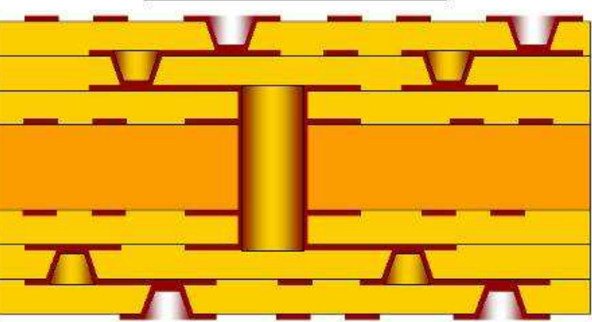
- **HDI Cost optimization – Design**

Base: pcb 160 mm x 110 mm / 2-4-2 HDI build up



Design
75 µm track width
75 µm spacing
burried vias drilled 0.3 mm
burried vias annular ring 150 µm
PTH Via drilled 0.3 mm
PTH Via annular ring 150 µm
micro vias drilled 0.1 mm
micro vias annular ring 75 µm
copper in pth 20 µm
pcb thickness 1.2 mm

Cost 100 %

Design
75 µm track width
75 µm spacing
burried vias drilled 0.2 mm
burried vias annular ring 125 µm
PTH Via drilled 0.2 mm
PTH Via annular ring 150 µm
micro vias drilled 0.1 mm
micro vias annular ring 60 µm
copper in pth 20 µm
pcb thickness 1.2 mm

Cost 113 %