

**HDI**

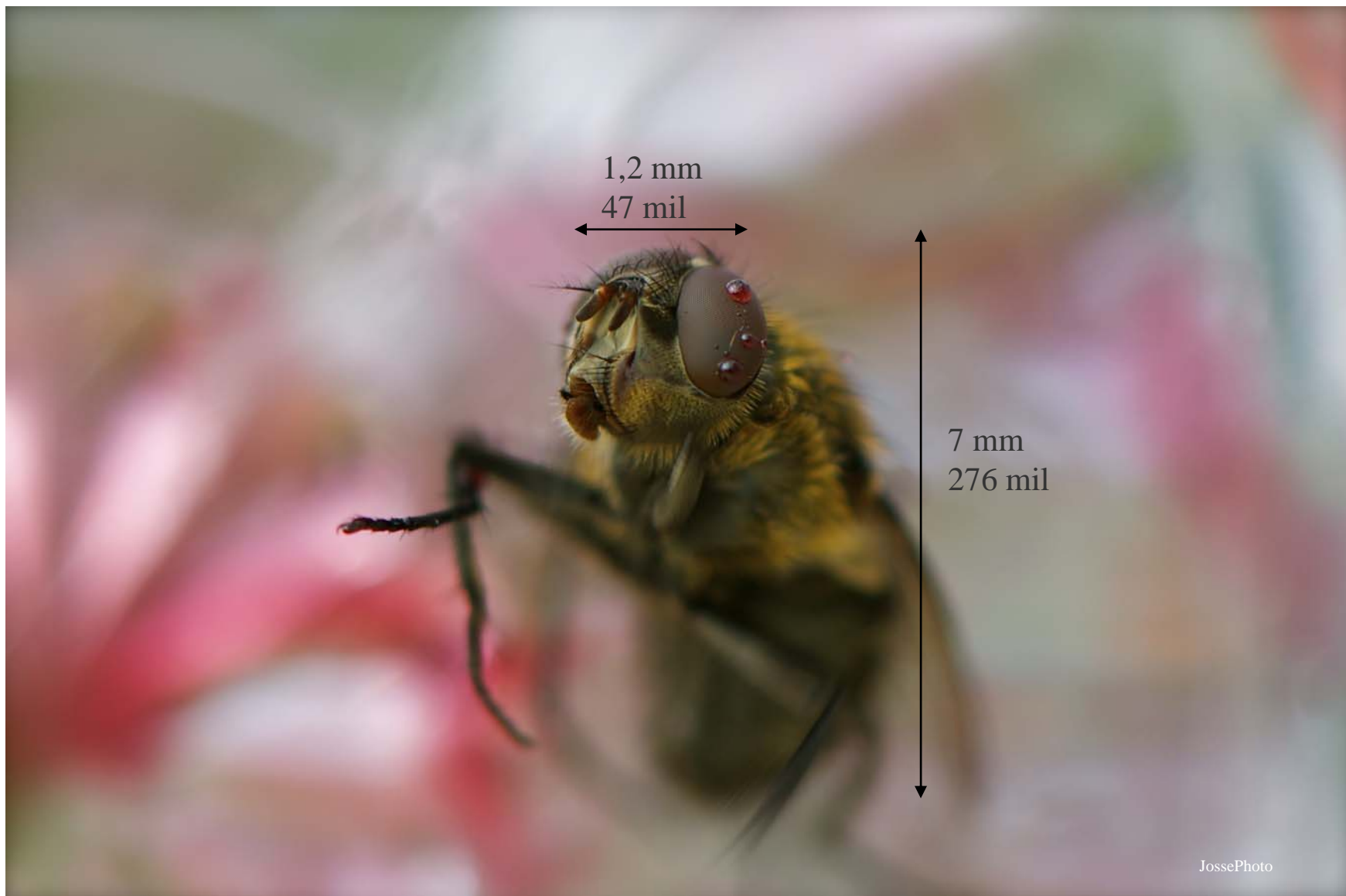
High Density Interconnect

**Hva vi ser i produksjon  
i dag.**

Josse -Sept. 2009

Jeg fotograferte krapylet i sommer da det lettet i fra en utspyttet morellstein.

Det røde på øynene er morell saft som sprutet opp idet den lettet.

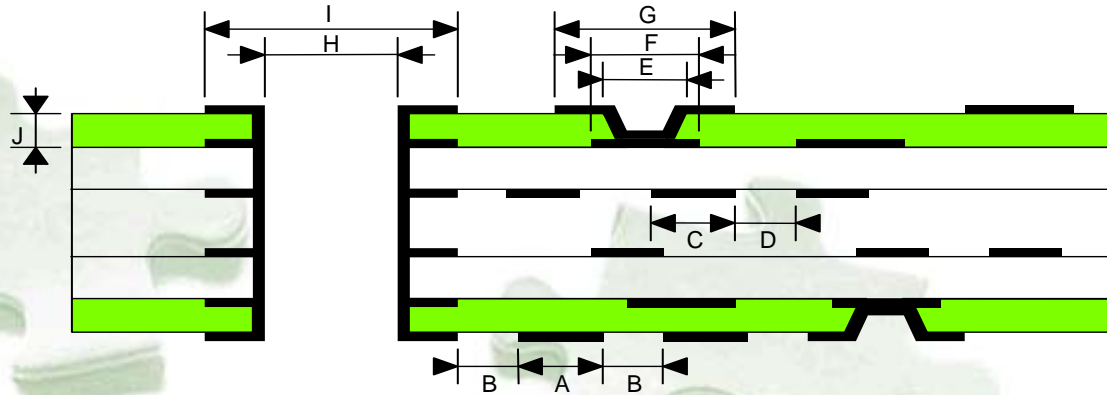


Mange insekter har fasettøyne. De er satt sammen av mange linser, som hver og en fungerer som et øye i seg selv. Hvert slikt øye er sekskantet og kan ha rundt 30 000 slike linser i hvert øye. Øyet er stort som et knappenålshode.

**Dette er HDI**



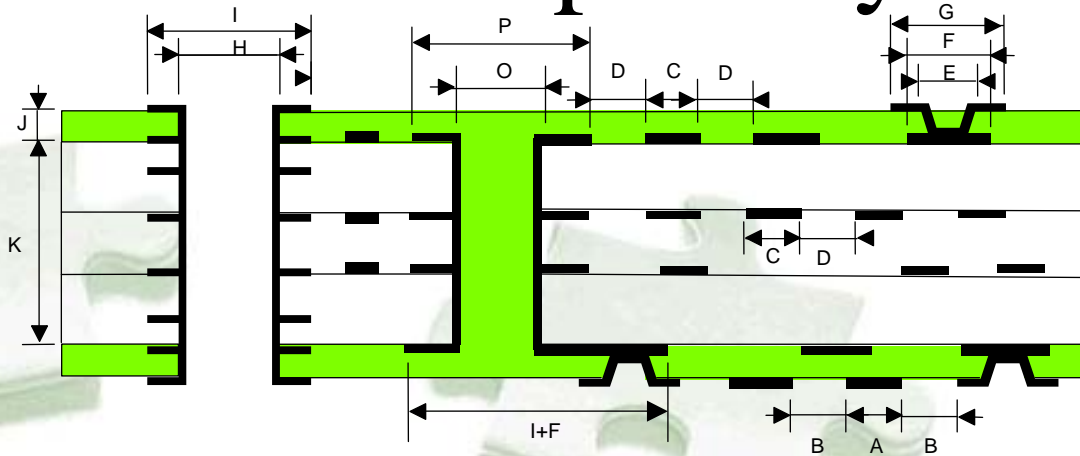
# HDI Capability



Symbol	Description	Production capability	Lead edge capability
	Base Copper	Cu 9~18um	Cu 3-18um
A	Minimum linewidth outerlayer	75um	75um
B	Minimum spacing outerlayer	75um	75um
C	Minimum linewidth innerlayer	75um	65um
D	Minimum spacing innerlayer	75um	75um
E	Microvia holesize	100um (min)	75(min)
F	Minimum Microvia landing pad	holesize + 200um	holesize + 150um
G	Minimum Microvia pad	holesize + 200um	holesize + 200um
H	Minimum drill size through hole	200um	200um
I	Minimum pad size through hole	drill size + 300um	drill size + 250um
J	Dielectric thickness	50~100um	50~125um

**HDI Design Rule (Type I, Per IPC2315)**

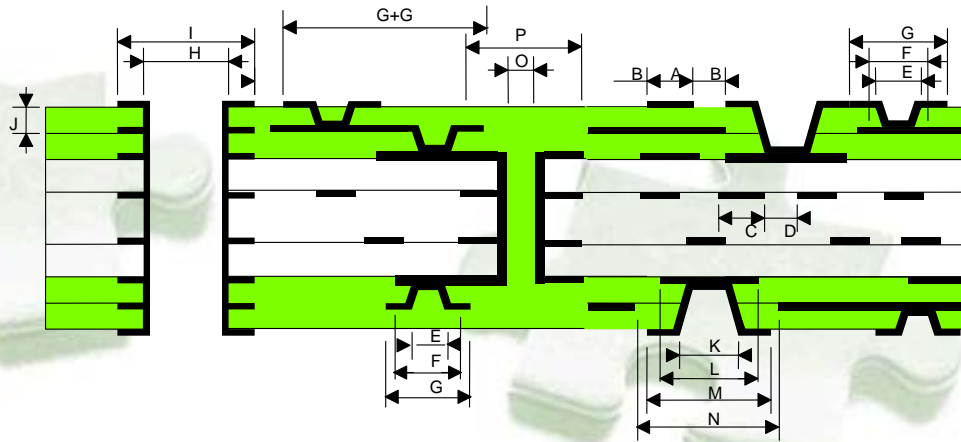
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E	Microvia holesize	100um (min)	75um (min)
F	Min Microvia landing pad	holesize + 200um	holesize + 150um
G	Min Microvia pad	holesize + 200um	holesize + 200um
H	Min drill size through hole	200um	200um
I	Min pad size through hole	drill size + 300um	drill size + 275um
J	Dielectric thickness	50~100um	50~150um
K	Max Core thickness	75mil	75mil
O	Min drill size buried hole	200 um	200 um
P	Min pad size buried hole	drill size + 300 um	drill size + 275 um

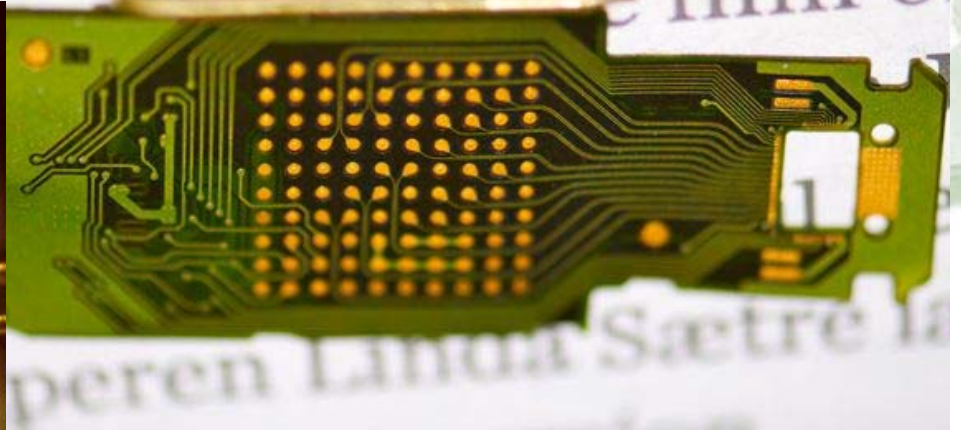
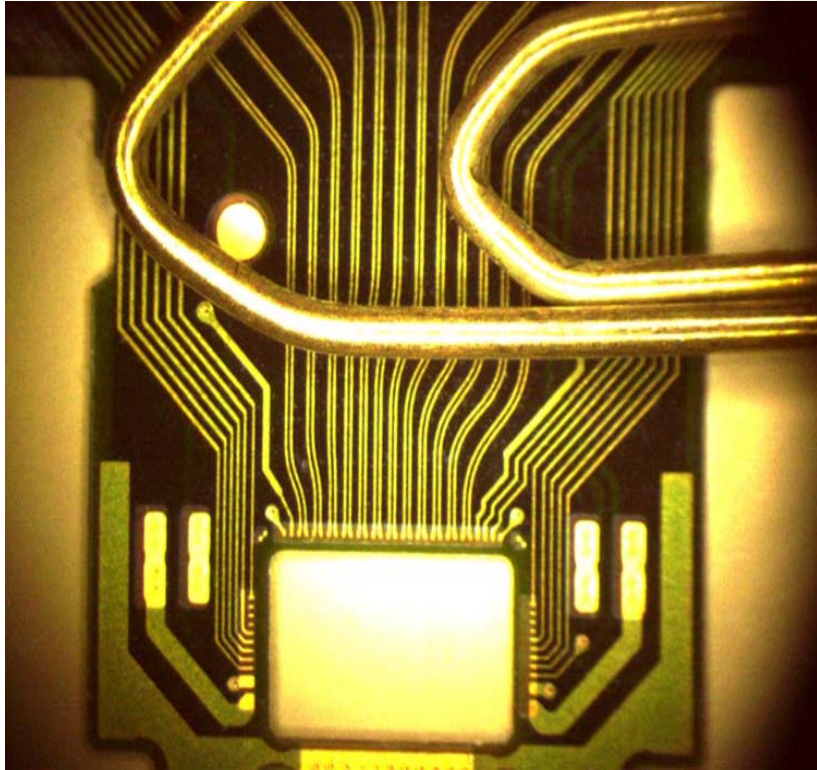
**HDI Design Rule (Type II, Per IPC2315)**

# HDI Capability



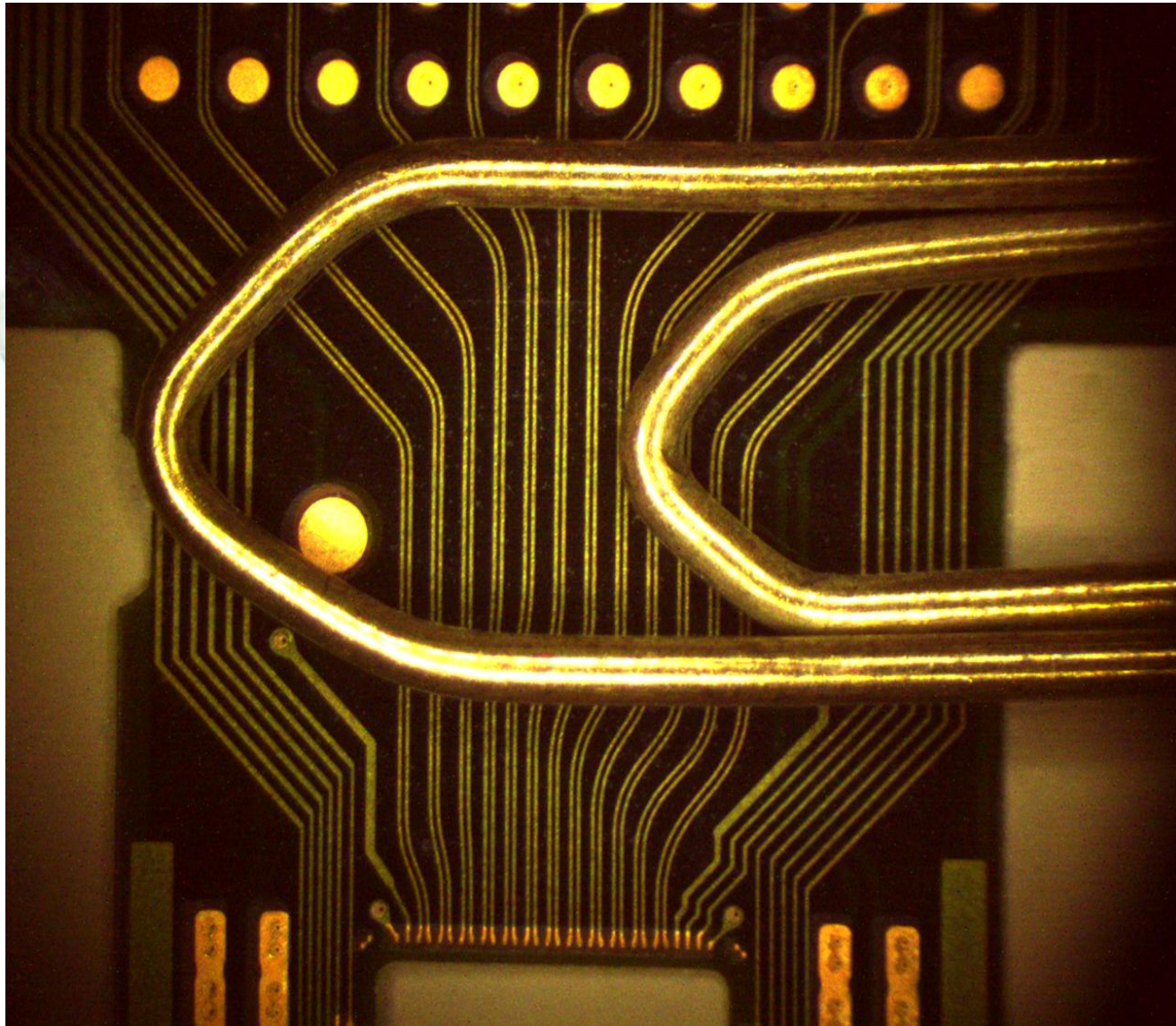
B	Min spacing outerlayer	75um	75um
C	Min linewidth innerlayer	75um	65um
D	Min spacing innerlayer	75um	75um
E	Microvia holesize	100um (min)	75um (min)
F	Min Microvia landing pad	holesize + 200um	holesize + 150um
G	Min Microvia pad	holesize + 200um	holesize + 200um
H	Min drill size through hole	200um	200um
I	Min pad size through hole	drill size + 300um	drill size + 275um
J	Dielectric thickness	50~100um	50~100um
K	Min Microvia hole	150um	150um
L	Min Microvia landing pad	holesize + 200um	holesize + 150um
M	Min Microvia pad	holesize + 200um	holesize + 200um
N	Minimum Microvia clearance pad	holesize + 350um	holesize + 325um
O	Min drill size buried hole	200um	200um
P	Min pad size buried hole	drill size + 300um	drill size + 275um

**HDI Design Rule (Type III, Per IPC2315)**

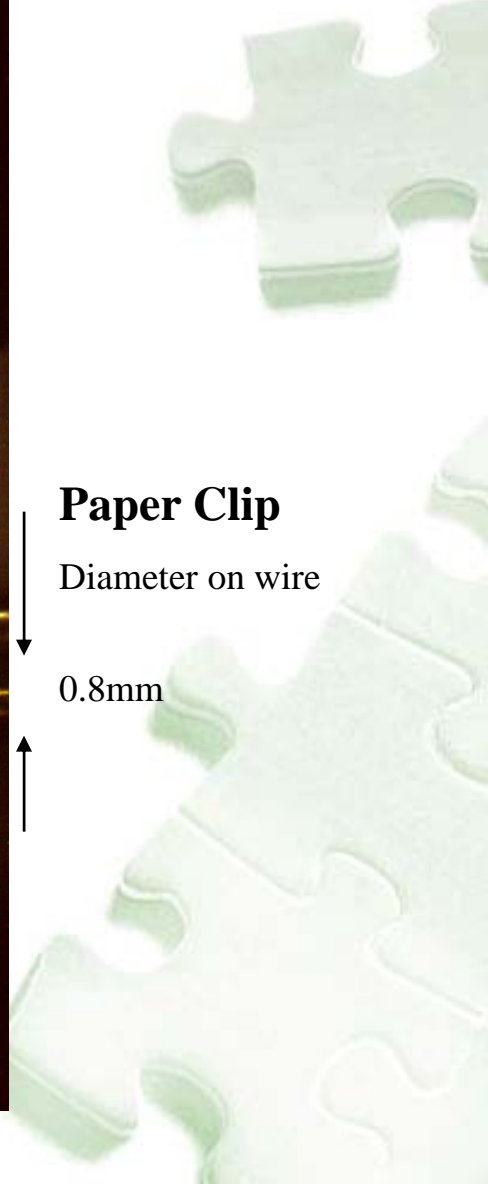


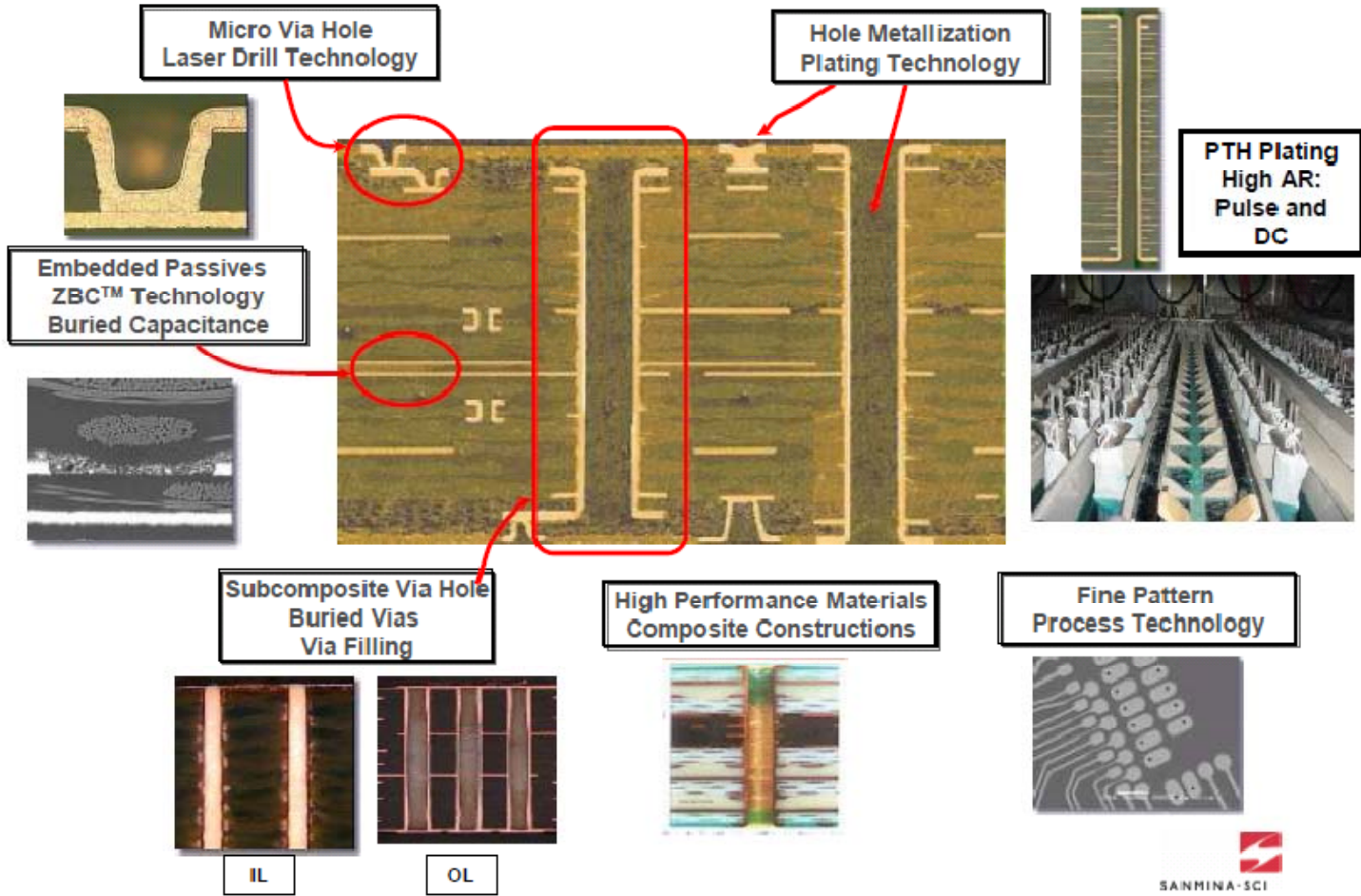
## HDI Flex

<b>Layers:</b>	2
<b>Size:</b>	42 x 17mm
<b>PCB thickness:</b>	50 um base, polyimide
<b>Track:</b>	40 um
<b>Gap:</b>	40 um
<b>Cu thickness:</b>	15 um
<b>Hole size:</b>	50 um



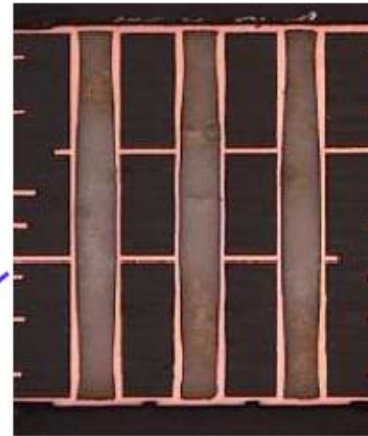
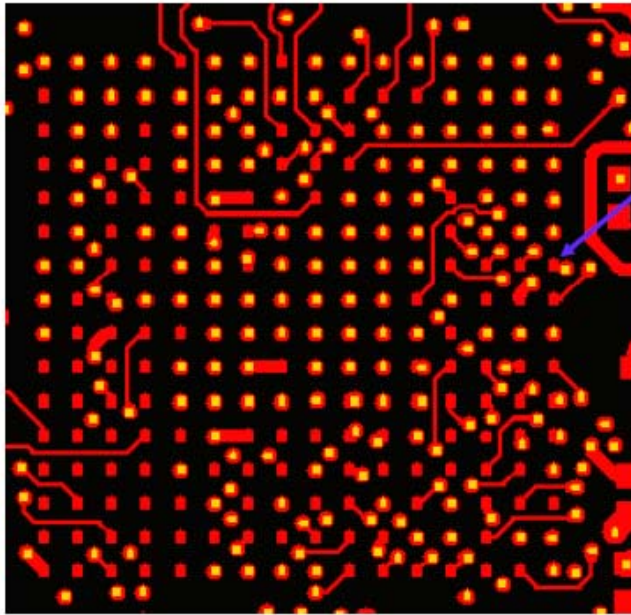
**Paper Clip**  
Diameter on wire  
0.8mm







# Filled Via in Pad

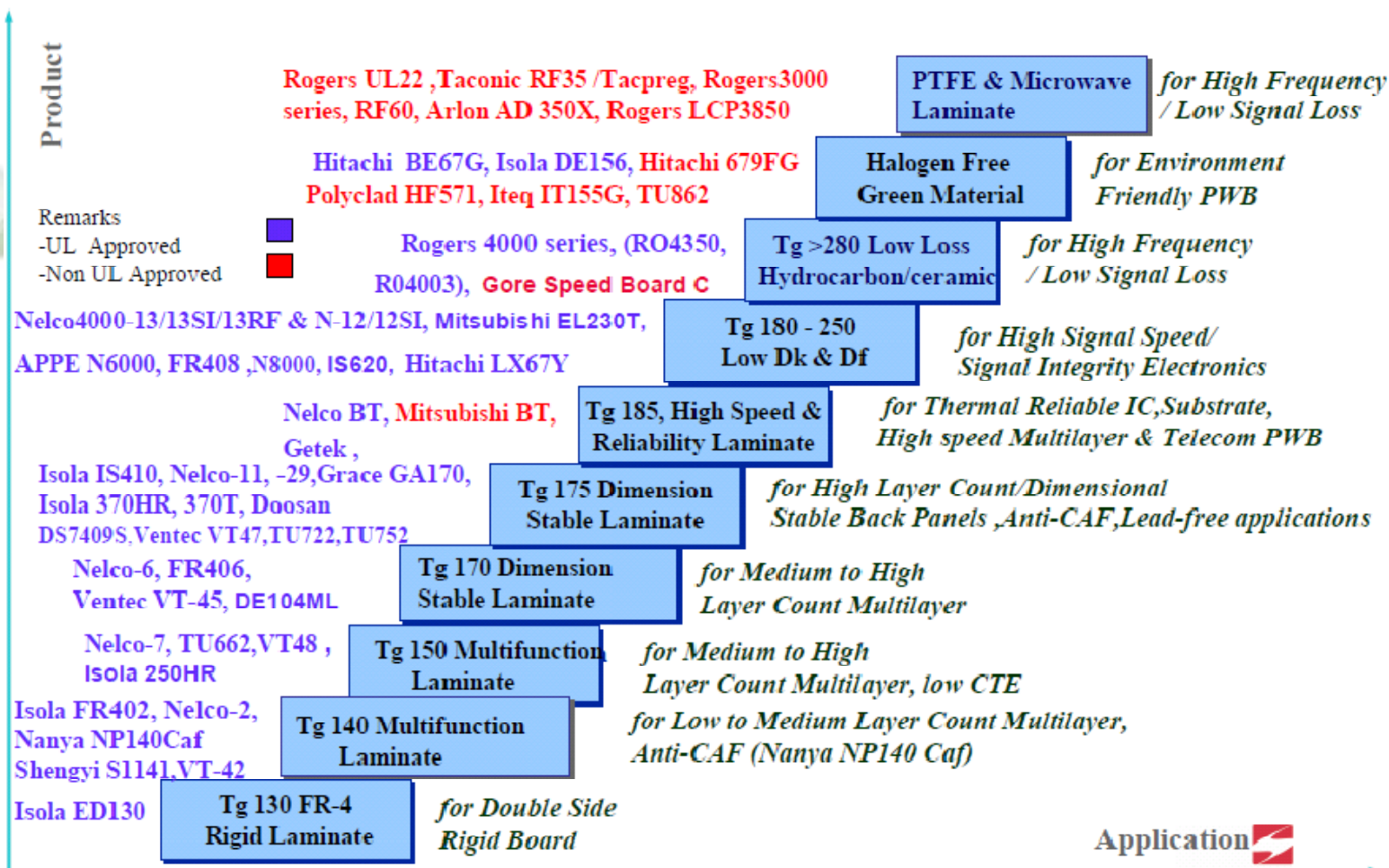


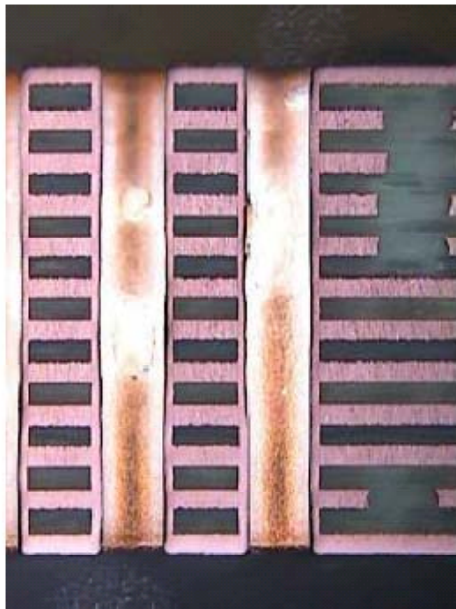
Cross section of plug vias



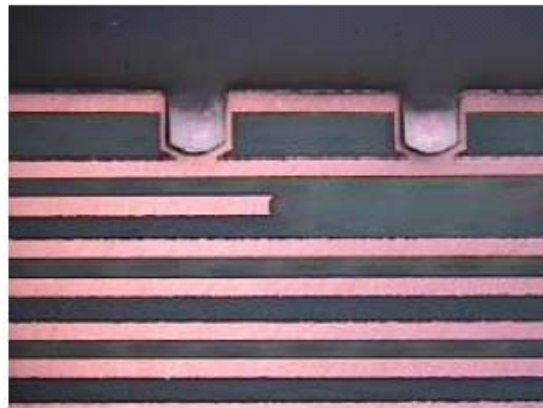
Cross section of plug vias

## Asia Laminate Spectrum

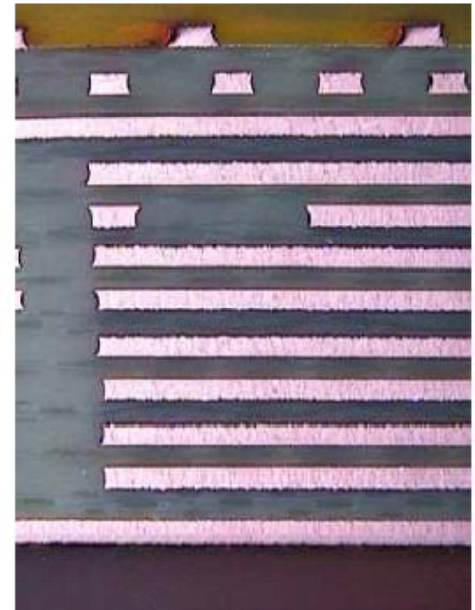




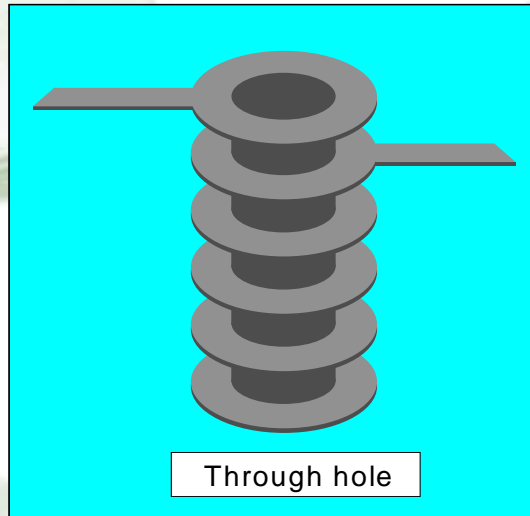
12 Layer PCB with 3 OZ INNER LAYER



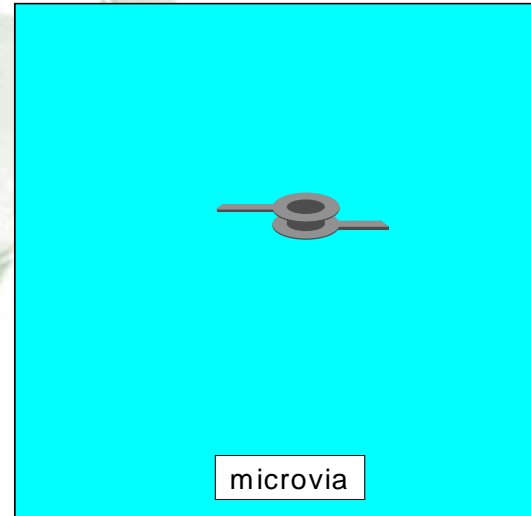
Heavy Copper Product with Control Depth  
Drill Hole Connection



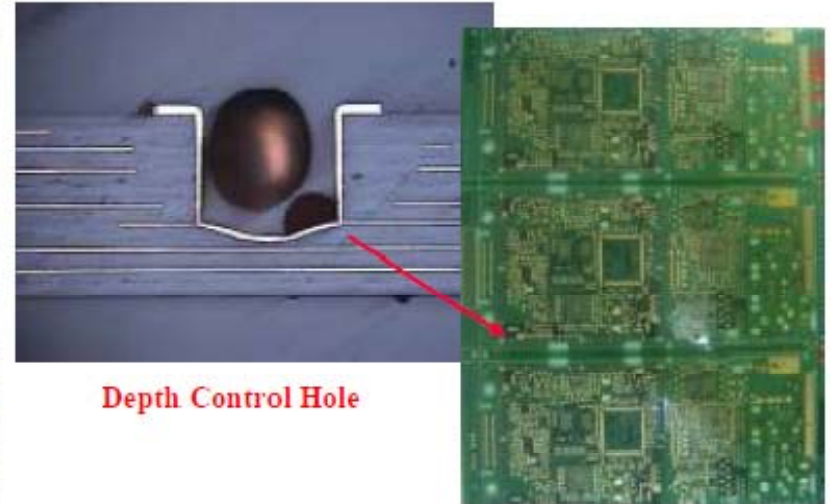
Typical Etch Factor (undercut / Copper  
Thickness) of  $< 0.5$



High Inductance



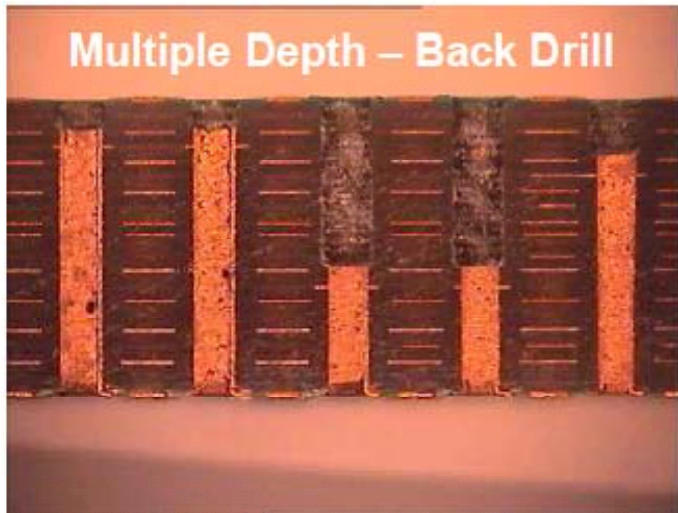
Lower Inductance



Depth Control Hole

e.g. Depth Control PCB

- **Drilling machine equipped with CBD (Contact Bit Drill) feature**
- **Machine Capability  $\pm 0.050\text{mm}$**
- **Every Hole drilled is 'zeroed' before drilling to desired depth.**  
(Zeroing achieved the moment Drill Bit touches Aluminum Entry)



## Product Example (above)

20 layers

Multiple Depths (3 per side)

Ending layer core thickness: 14 mil

Primary drill size: 27.6 mils

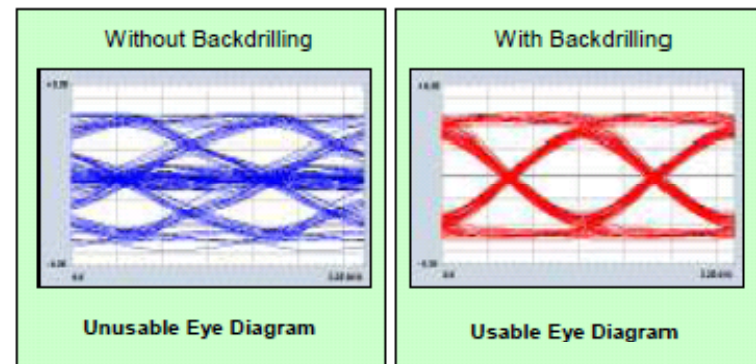
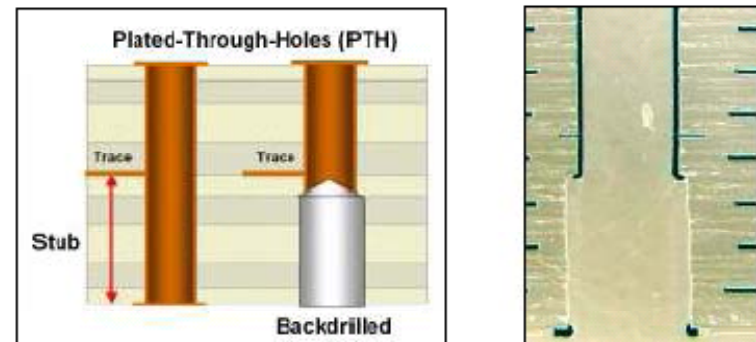
Back drill size: 33.5 mils

Dielectric spacing : minimum 8 mils

Depth Tolerance : +/- .004

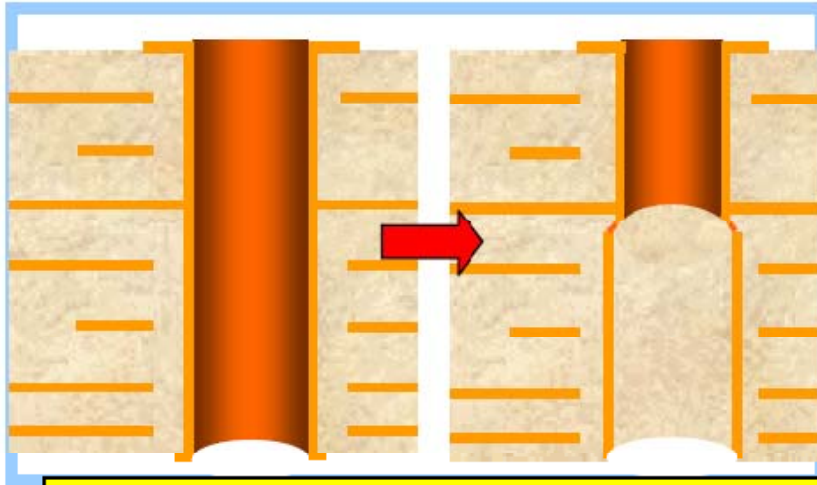
Repeatability : +/- .001

Backdrilling eliminates detrimental plated-through-hole (PTH) via stub effects that distort signals passing through them



6.25 Gb/s Data Rate

## Some key advantages to stub removal of plated holes include:



Applied as controlled depth NC Drilling



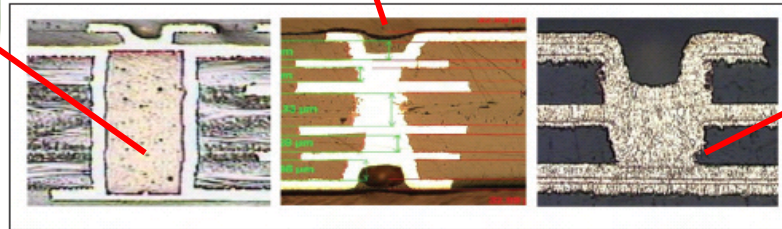
Improvement in the frequency domain

- Reduced deterministic jitter
- Lower bit error rate (BER)
- Less signal attenuation with improved impedance matching
- Increased channel bandwidth
- Reduced EMI/EMC radiation from the stub end
- Reduced excitation of resonance modes
- Reduced via-to-via crosstalk

We see this...  
but not often

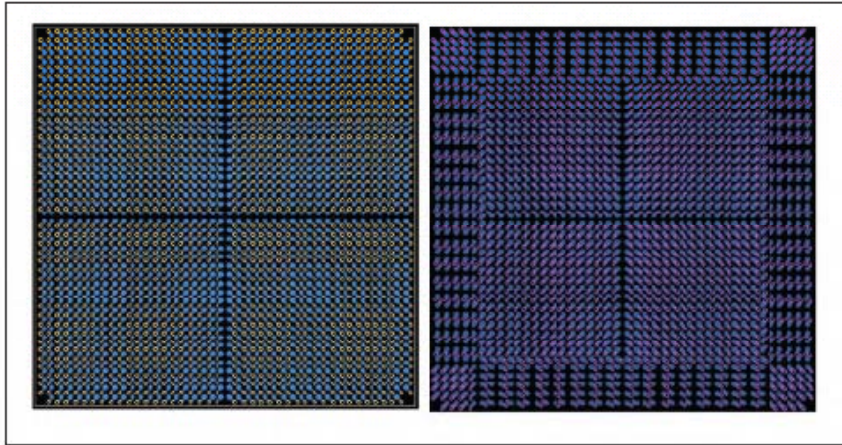
We dont see this,  
and we do not recommend it.

We dont see this,  
and we do not recommend it.

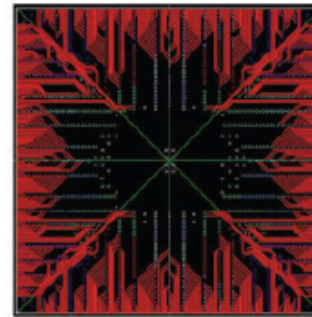
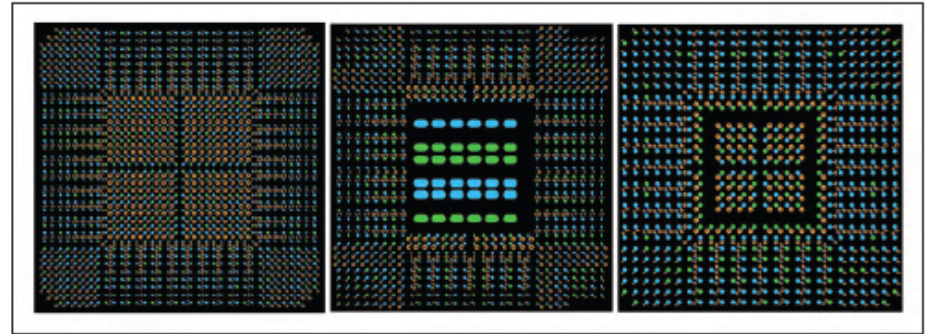


**Filled vias, on which the stacked vias are built, can be filled by three techniques:**

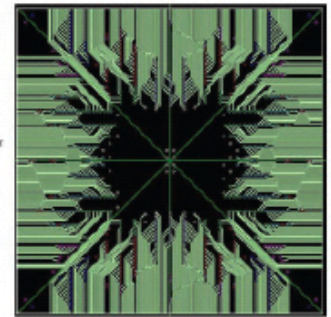
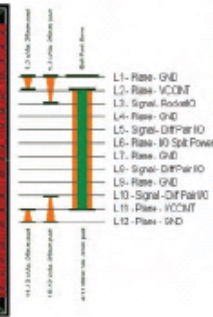
- Conductive paste and cap plating
- Non-conductive filling, metallization, and cap plating
- Special high-throw electroplating that will fill the via



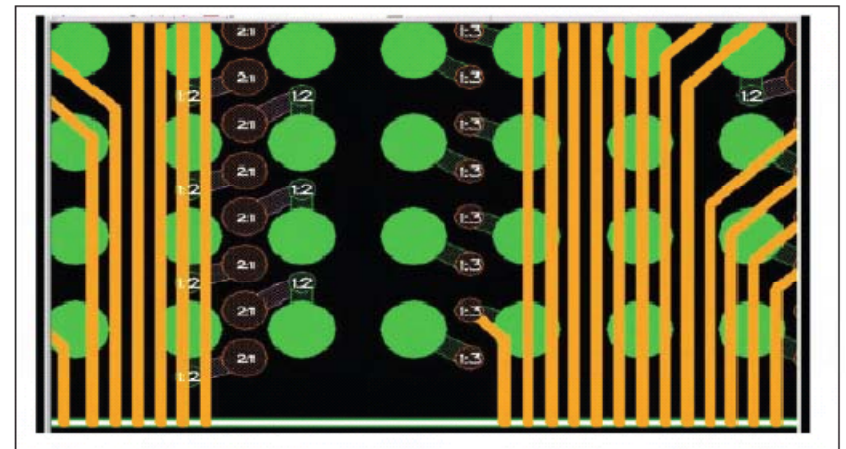
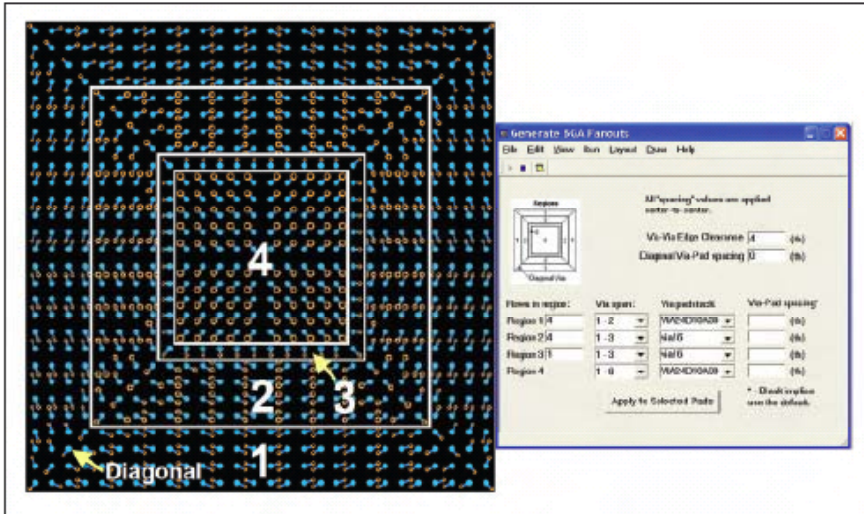
Orderly, structure via fan out placement, gives an optional routing in lined up channels. Different via types kept in sections.



L3-Signal - Rocket IO



L5-Signal - Diff Pair IO

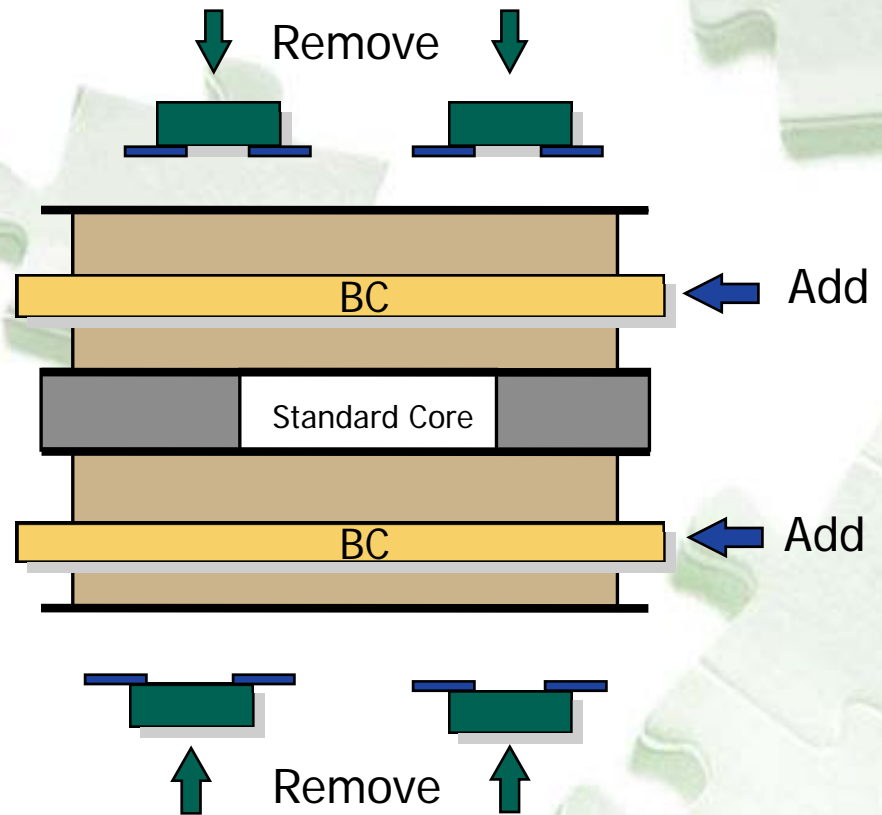




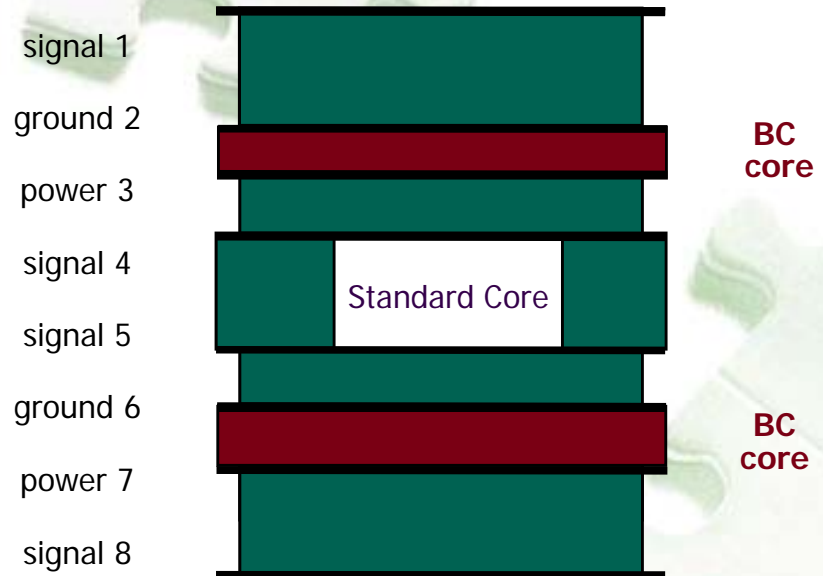
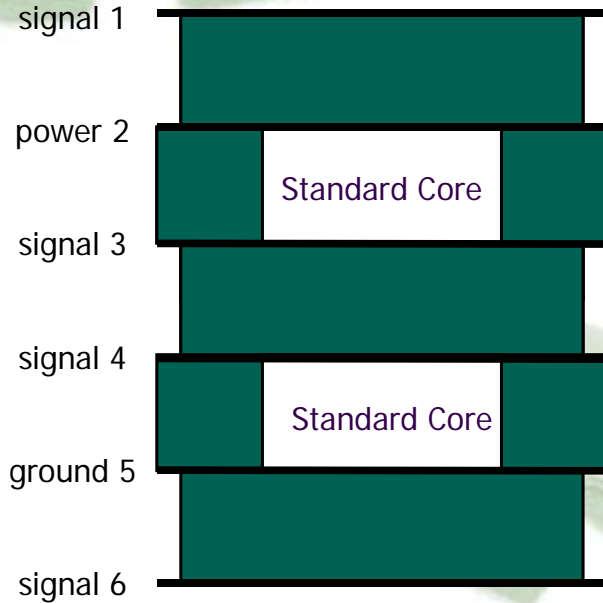
**Buried  
Capacitance**

## *A Very Simple Idea*

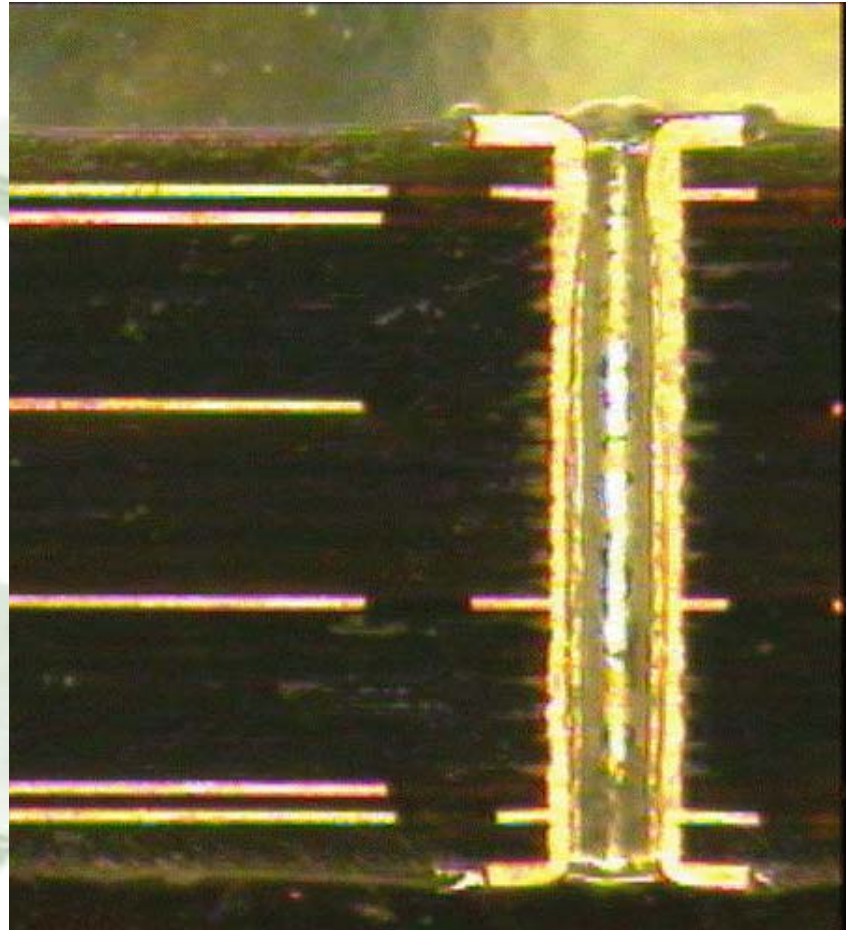
Use the Power and Ground Planes to Form Buried Capacitance™ (BC) Planes Within the PCB, and Remove Most of the Bypass Capacitors



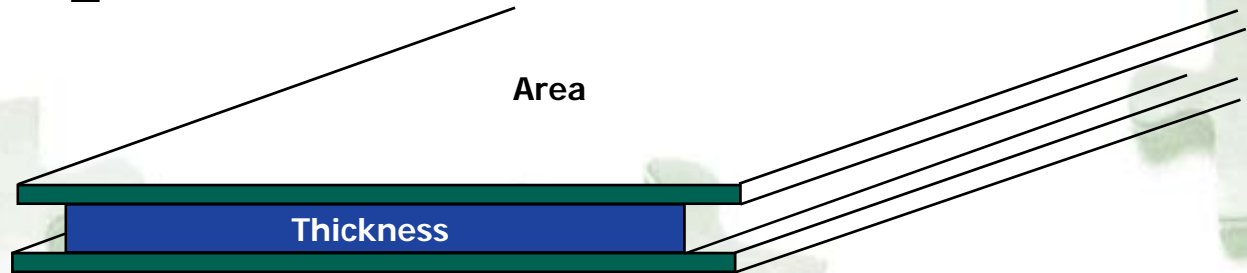
# Conversion is Simple with Capacitive Layers



# BC Photomicrograph



# Capacitance Calculation



$C = A\epsilon D/t$  where

C - is total capacitance

A - is the area per sq. inch of the plane (or split plane)  
attached to the active devices

$\epsilon$  - is the dielectric constant of the dielectric material

D - is a constant (225)

t - is the thickness of the dielectric material in mils

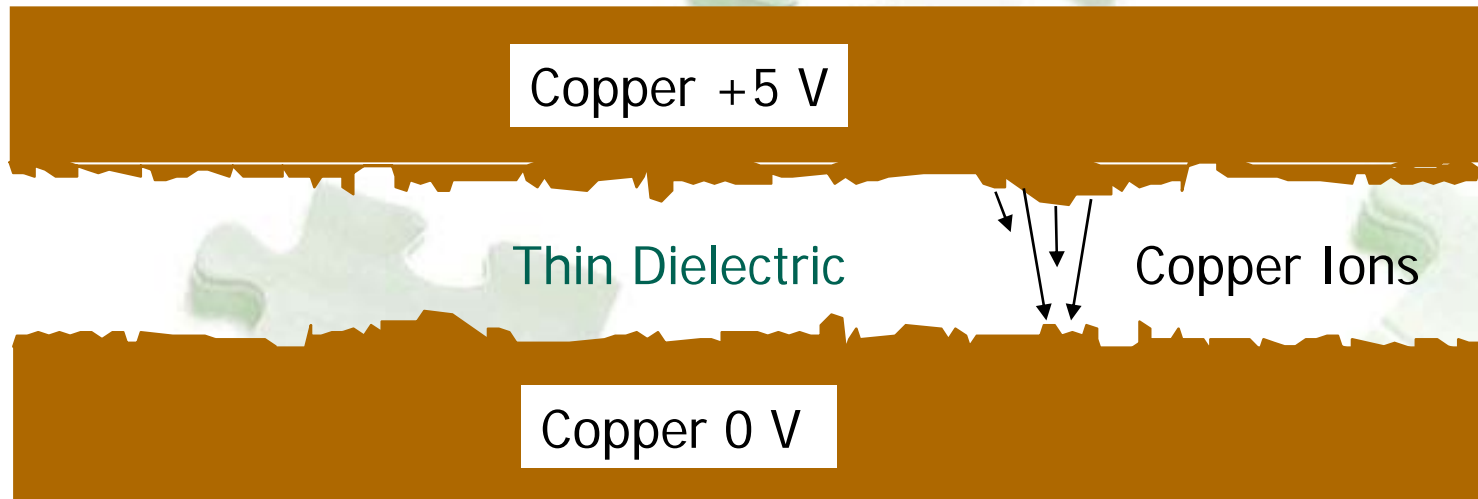
Example:  $(10'' \times 10'' \text{ PCB}) * 2 \text{ Planes} * 4.5 * 225 / 2$

= 101,250 Picofarads, or **.1  $\mu\text{F}$**

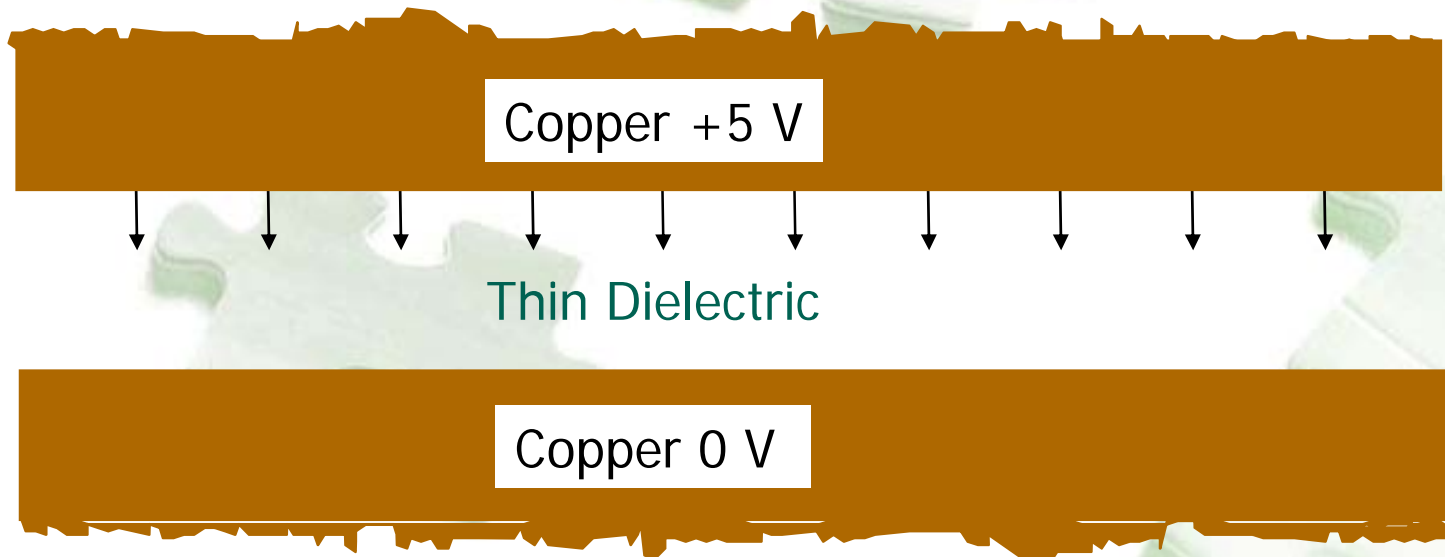
May not be applicable on small area parts

**Available dielectric thickness 50  $\mu\text{m}$  and 25  $\mu\text{m}$**

# Electromigration of Copper Due to Temperature and Humidity



BC Has Flat Internal Surfaces to  
Distribute the Voltage...and is Tested at  
500 VDC

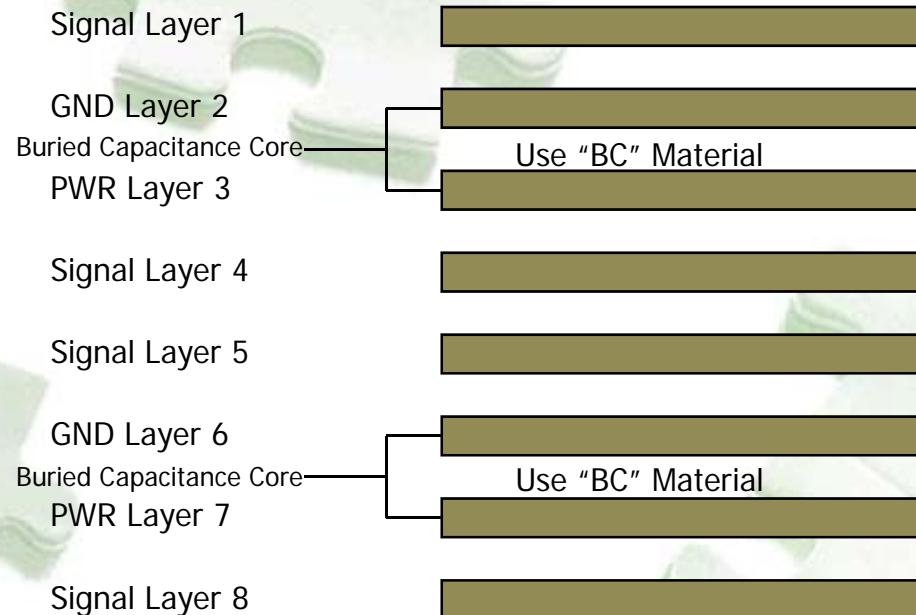


# Specifying BC Constructions

## Print Notes:

In addition to all other notes, copper weight, impedance, etc., the following specific notes should be included.

1. All "BC" images to be Hi-Pot tested at 500 VDC after layer etch
2. Final Hi-Pot test required prior to packaging 500 VDC



## LUNCH on a Melon Skin



**Elmatica**  
*Purchasing PCBs is a puzzle!*



**Elmatica**  
*Purchasing PCBs is a puzzle!*



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*Purchasing PCBs is a puzzle!*



**Elmatica**  
*Purchasing PCBs is a puzzle!*



**Elmatica**  
*Purchasing PCBs is a puzzle!*





Vi kan se hvor Bugatti har hentet inspirasjon fra



Denne forsøkte å stikke av, men jeg hang meg på....

Nu gleder vi oss til fortsettelsen av denne dagens foredrag..



**The End**