



A Practical Guide to PCB layout of DDR2

Quadra Solutions





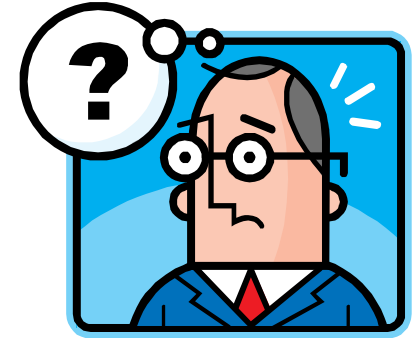
At a supermarket somewhere near where you live ...

- The Why, When, What & How of DDR2
- Planning and Preparation
 - Understanding the requirements
 - Setting up rules and constraints
- Placement and Routing Implementation
 - Developing an effective layout strategy
 - Using tools to efficiently implement the design
- Checking & Verification
 - Design rules
 - Electrical characteristics



Why, When, What & How of DDR2

- Why Use DDR2?
 - Often the only cost effective technology available
 - Because other devices in the design require it
- When should I start planning?
 - As soon as possible
 - It will always take longer than you anticipate!
 - When you believe you might have a problem....
- What do I need to do?
 - Conform to a set of Rules and Constraints
 - length, skew, crosstalk, timing and topology
- How?
 - Read the chip vendor's Datasheet and Reference Notes
 - Follow the practical guidelines in this presentation



What is driving Change?

- Customer demand

- Smaller
- Faster
- Better
- Cheaper



- Consequential impact

- High density, fine pitch devices
- Highly automated manufacturing

- Negative effects (on design) include

- High speed clocks and fast edge rates
- Increase in ambient RF
- E.M.C. emissions and susceptibility
- Thermal dissipation
- ??



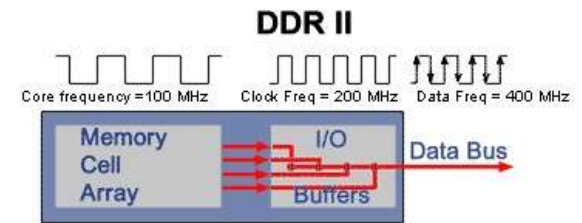
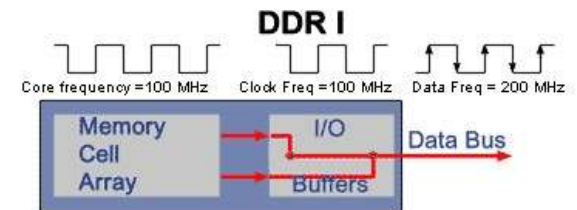
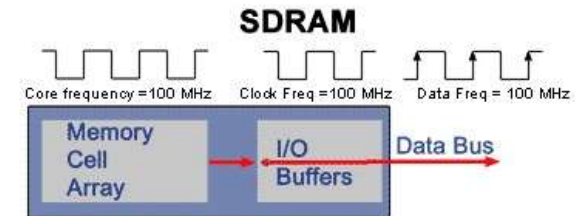
Chip Vendors now set the Agenda...

- Design Engineers use what is available
 - Trade Cost v. Functionality
 - Have to adopt new technologies and standards
- Implementation cost is increasing
 - Layer count
 - High speed interfaces
 - Power and decoupling
 - Design time
- Interconnect technologies are now driving PCB Layout
 - PCI, PCI Express
 - USB
 - DDR2
 - Etc..



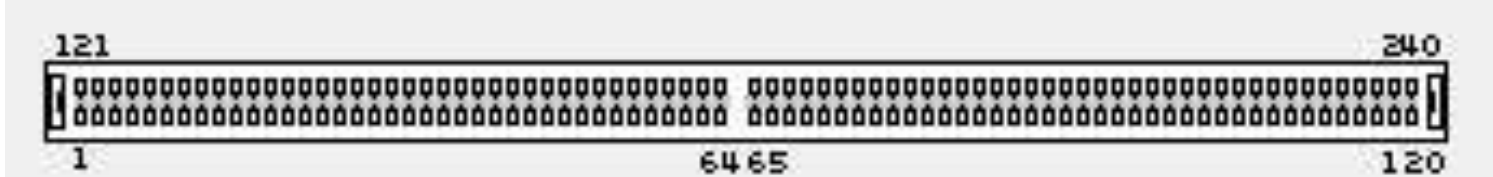
DDR2 in a nutshell

- DDR2 = Double Data Rate 2
 - Clocked on both the rising and falling edge, at double the core rate
- DDR2 allows:
 - higher bus speed
 - lower power consumption
 - 64 bit bus width
- Packaging
 - BGA devices
 - DIM Modules
- Defined Bus Structures
 - Data group
 - Address / CMD group
 - Control group
 - Clock group



Typical DDR2 DIMM

- Pin out



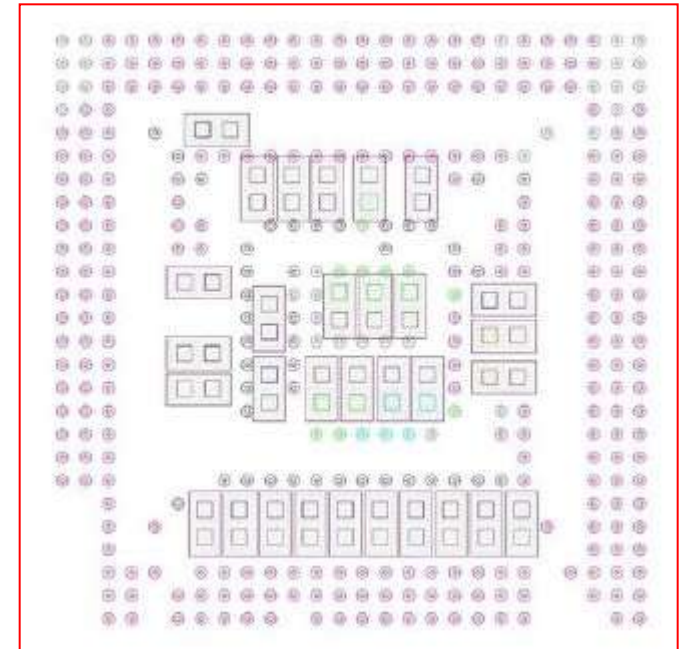
- Key

A0 to A13 Address input
BA0, BA1 Bank select address
DQ0 to DQ63 Data input/output
/RAS Row address strobe command
/CAS Column address strobe command
/WE Write enable
/CS0, /CS1 Chip select
CKE0, CKE1 Clock enable
CK0 to CK2 Clock input
/CK0 to /CK2 Differential clock input
DQS0 to DQS7, /DQS0 to /DQS7 Input and output data
DM0 to DM7 Input mask
SCL Clock input for SPD
SDA Data input/output for SPD
SA0 to SA2 Serial address input
VDD Power for internal circuit
VDDQ Power for DQ circuit
VDDSPD Power for serial EEPROM
VREF Input reference voltage
VSS Ground
ODT0, ODT1 ODT control
NC No Connection

Pin #	Description	Pin #	Description	Pin #	Description	Pin #	Description	Pin #	Description	Pin #	Description
1	VREF	41	VSS	81	DQ33	121	VSS	161	NC	201	VSS
2	VSS	42	NC	82	VSS	122	DQ4	162	NC	202	DM4
3	DQ0	43	NC	83	/DQS4	123	DQ5	163	VSS	203	NC
4	DQ1	44	VSS	84	DQS4	124	VSS	164	NC	204	VSS
5	VSS	45	NC	85	VSS	125	DM0	165	NC	205	DQ38
6	/DQS0	46	NC	86	DQ34	126	NC	166	VSS	206	DQ39
7	DQS0	47	VSS	87	DQ35	127	VSS	167	NC	207	VSS
8	VSS	48	NC	88	VSS	128	DQ6	168	NC	208	DQ44
9	DQ2	49	NC	89	DQ40	129	DQ7	169	VSS	209	DQ45
10	DQ3	50	VSS	90	DQ41	130	VSS	170	/VDDQ	210	VSS
11	VSS	51	/VDDQ	91	VSS	131	DQ12	171	CKE1	211	DM5
12	DQ8	52	CKE0	92	/DQS6	132	DQ13	172	VDD	212	NC
13	DQ9	53	VDD	93	DQS5	133	VSS	173	NC	213	VSS
14	VSS	54	NC	94	VSS	134	DM1	174	NC	214	DQ46
15	/DQS1	55	NC	95	DQ42	135	NC	175	/VDDQ	215	DQ47
16	DQS1	56	/VDDQ	96	DQ43	136	VSS	176	A12	216	VSS
17	VSS	57	A11	97	VSS	137	CK1	177	A9	217	DQ52
18	NC	58	A7	98	DQ48	138	/CK1	178	VDD	218	DQ53
19	NC	59	VDD	99	DQ49	139	VSS	179	A8	219	VSS
20	VSS	60	A5	100	VSS	140	DQ14	180	A6	220	CK2
21	DQ10	61	A4	101	SA2	141	DQ15	181	/VDDQ	221	/CK2
22	DQ11	62	/VDDQ	102	NC	142	VSS	182	A3	222	VSS
23	VSS	63	A2	103	VSS	143	DQ20	183	A1	223	DM6
24	DQ16	64	VDD	104	/DQS6	144	DQ21	184	VDD	224	NC
25	DQ17	65	VSS	105	DQS6	145	VSS	185	CK0	225	VSS
26	VSS	66	VSS	106	VSS	146	DM2	186	/CK0	226	DQ54
27	/DQS2	67	VDD	107	DQ50	147	NC	187	VDD	227	DQ55
28	DQS2	68	NC	108	DQ51	148	VSS	188	A0	228	VSS
29	VSS	69	VDD	109	VSS	149	DQ22	189	VDD	229	DQ60
30	DQ18	70	A10/AP	110	DQ56	150	DQ23	190	BA1	230	DQ61
31	DQ19	71	BA0	111	DQ57	151	VSS	191	/VDDQ	231	VSS
32	VSS	72	/VDDQ	112	VSS	152	DQ28	192	/RAS	232	DM7
33	DQ24	73	/WE	113	/DQS7	153	DQ29	193	/CS0	233	NC
34	DQ25	74	/CAS	114	DQS7	154	VSS	194	/VDDQ	234	VSS
35	VSS	75	/VDDQ	115	VSS	155	DM3	195	ODT0	235	DQ62
36	/DQS3	76	/CS1	116	DQ58	156	NC	196	A13	236	DQ63
37	DQS3	77	DDT1	117	DQ59	157	VSS	197	VDD	237	VSS
38	VSS	78	/VDDQ	118	VSS	158	DQ30	198	VSS	238	/VDDSPD
39	DQ26	79	VSS	119	SDA	159	DQ31	199	DQ36	239	SA0
40	DQ27	80	DQ32	120	SCL	160	VSS	200	DQ37	240	SA1

DDR2 - Key Design Considerations

- Timing is Critical
 - Achieved by matching track Length / signal Delay
- Termination
 - Internal
 - On Die Termination
 - Value, strength
 - External
 - Series damping resistors
 - Parallel resistors to VTT
 - Differential terminators
 - Compensation capacitors
- Decoupling
 - As defined in vendor datasheet



Planning Considerations

- Establish Design Rules

- Area rules
- Spacing classes
- Impedance controlled tracks
- Differential pairs

Routing Class	Layer	Byte Lane 0	Byte Lane 0 STMB	Byte Lane 1	Byte Lane 2	Byte Lane 3	Byte Lane 4	Byte Lane 5	Byte Lane 6	Byte Lane 7
(Default)	(Default)	25.000	25.000	25.000	25.000	25.000	25.000	25.000	25.000	25.000
Byte Lane 0	(Default)	10.000	10.000	25.000	25.000	25.000	25.000	25.000	25.000	25.000
Byte Lane 0 STMB	(Default)									
Byte Lane 1	(Default)			10.000	25.000	25.000	25.000	25.000	25.000	25.000
Byte Lane 2	(Default)				10.000	25.000	25.000	25.000	25.000	25.000
Byte Lane 3	(Default)					10.000	25.000	25.000	25.000	25.000
Byte Lane 4	(Default)						10.000	25.000	25.000	25.000
Byte Lane 5	(Default)							10.000	25.000	25.000
Byte Lane 6	(Default)								10.000	25.000
Byte Lane 7	(Default)									10.000

- Layer Stack

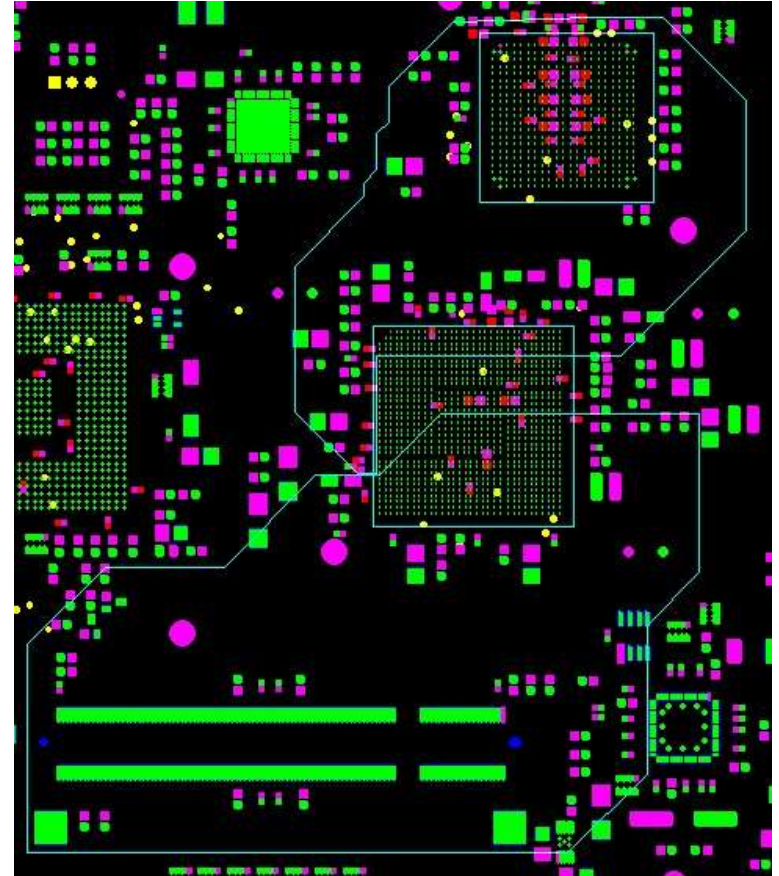
- Construction and materials
- Power and Reference Plane definitions
- Via types and interconnects

- Other 'To Do' Items

- Assign 'ref_voltage' attributes
- Run the Field Solver



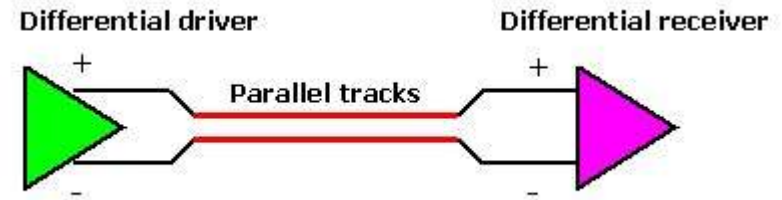
- Define alternate Design Rule sets
 - Over high pin density devices
 - Surrounding byte lanes
- Define Placement keepout areas
 - Manufacturing limits for placement
 - Clear channels for length management
- Spacing Classes
 - Enable multiple spacing assignments
 - Within a Class
 - Between Classes
 - To all Unclassed nets



Impedance Calculations

DDR2 Data group

- Single Ended
 - Target 50 ohm
- Differential
 - Target 90 ohm

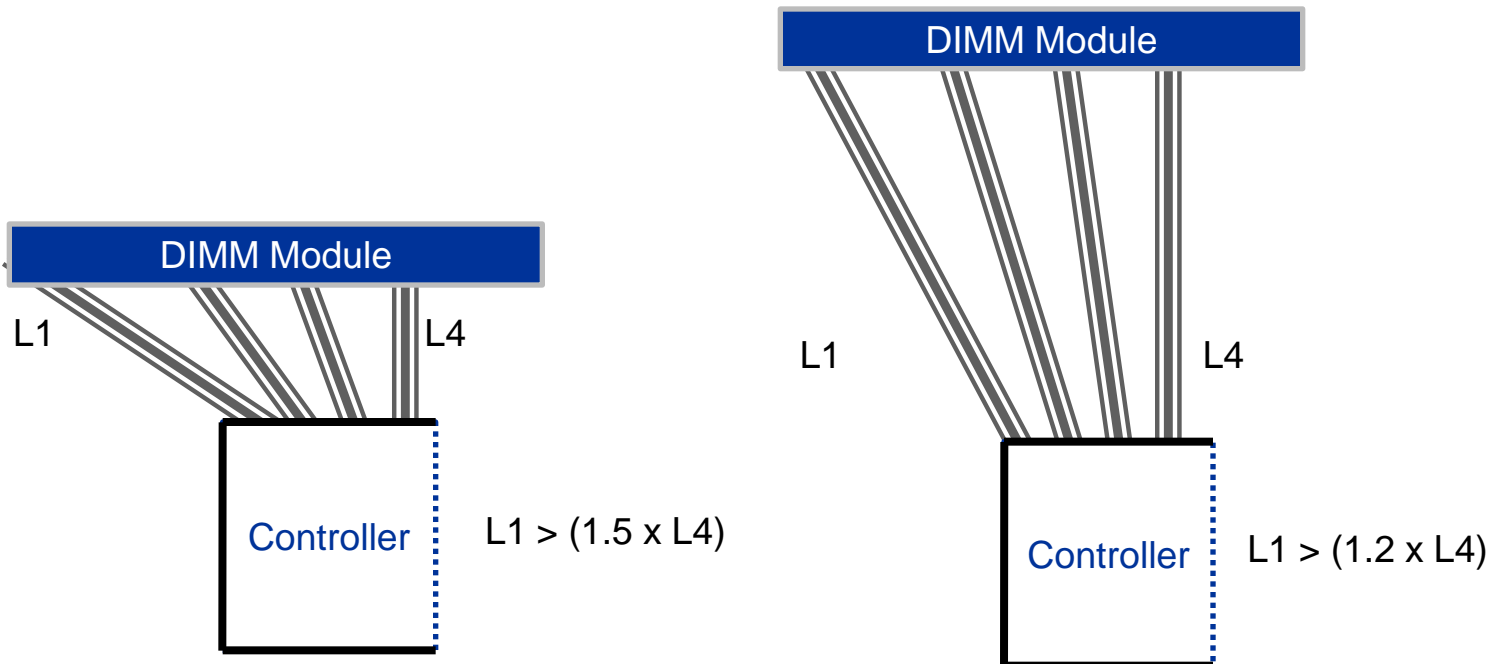


Layer Stack		Z0 Planning		Zdiff Planning	
Impedance Templates					
Impedance Template 1		Add...		Delete	
	Type	Width (mm)	Z0 (Ohm)	Velocity (mm/ps)	
All			50.00		
1 (Top Elec)	Signal	0.091	25.00	0.150	
3 (GND)	Signal	0.868		0.158	
5 (Sig 1)	Signal	0.084		0.141	
7 (VCC 1)	Signal	0.172		0.141	
9 (VCC 2)	Signal	0.173		0.141	
11 (Sig 2)	Signal	0.063		0.141	
13 (GND 2)	Signal	0.890		0.157	
15 (Bottom Elec)	Signal	0.175	25.00	0.151	

Layer Stack		Z0 Planning		Zdiff Planning			
Impedance Templates							
Impedance Template 1		Add...		Delete			
	Type	Width (mm)	Spacing (mm)	Z_diff (Ohm)	Z_odd (Ohm)	Z_even (Ohm)	Z_0
All			0.102	100.00			
1 (Top Elec)	Signal	0.081		50.00	25.11	28.15	
3 (GND)	Signal	1.341		50.00	25.00	46.40	
5 (Sig 1)	Signal	0.250		50.00	25.03	31.19	
7 (VCC 1)	Signal	0.411		50.00	25.00	37.42	
9 (VCC 2)	Signal	0.412		50.00	25.02	37.58	
11 (Sig 2)	Signal	0.200		50.00	25.02	30.36	
13 (GND 2)	Signal	0.110			50.08	159.43	
15 (Bottom Elec)	Signal	0.150		50.00	25.08	29.67	

Placement of Core Components

- Length matching between Byte Lanes may necessitate placing core devices further apart to simplify tuning



- Signals from different groups are broken down into 'Byte Lanes'
 - Data
 - Control
 - Differential strobes
- Examples
 - Byte Lane 0
 - MADQ(7:0)
 - MA-DM0
 - MADQS0
 - MADQS0
 - Byte Lanes 1 - 7
 - Repeated
 - “” “”
 - “” “”
 - “” “”
- Byte Lanes must be routed together
 - On the same layer
 - Within specific constraints



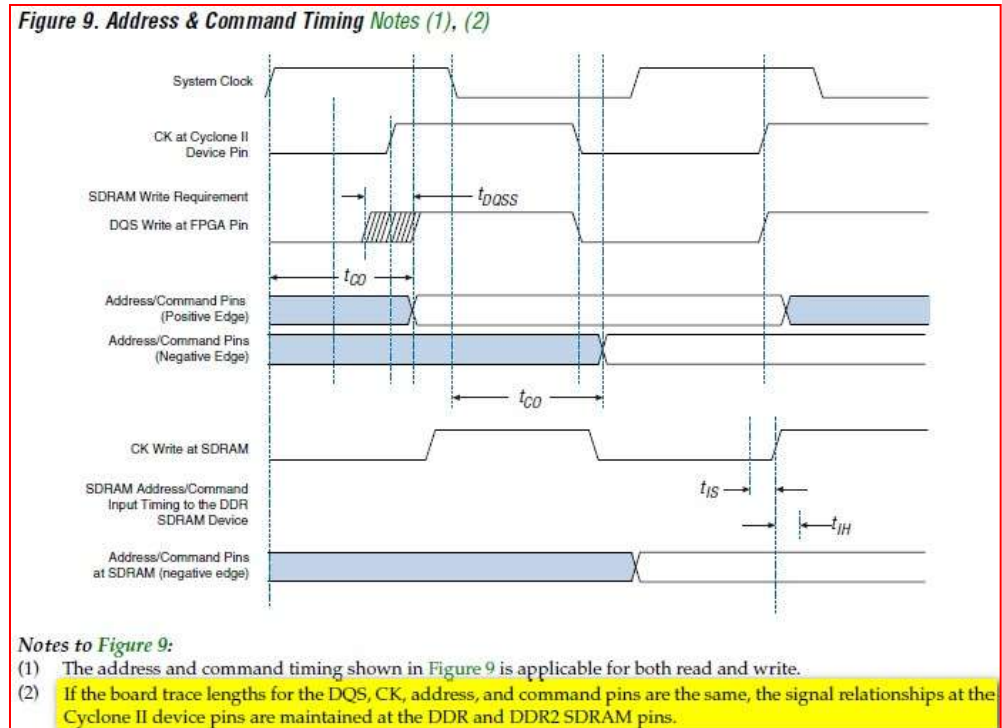
Additional Design Guidelines – A Sample



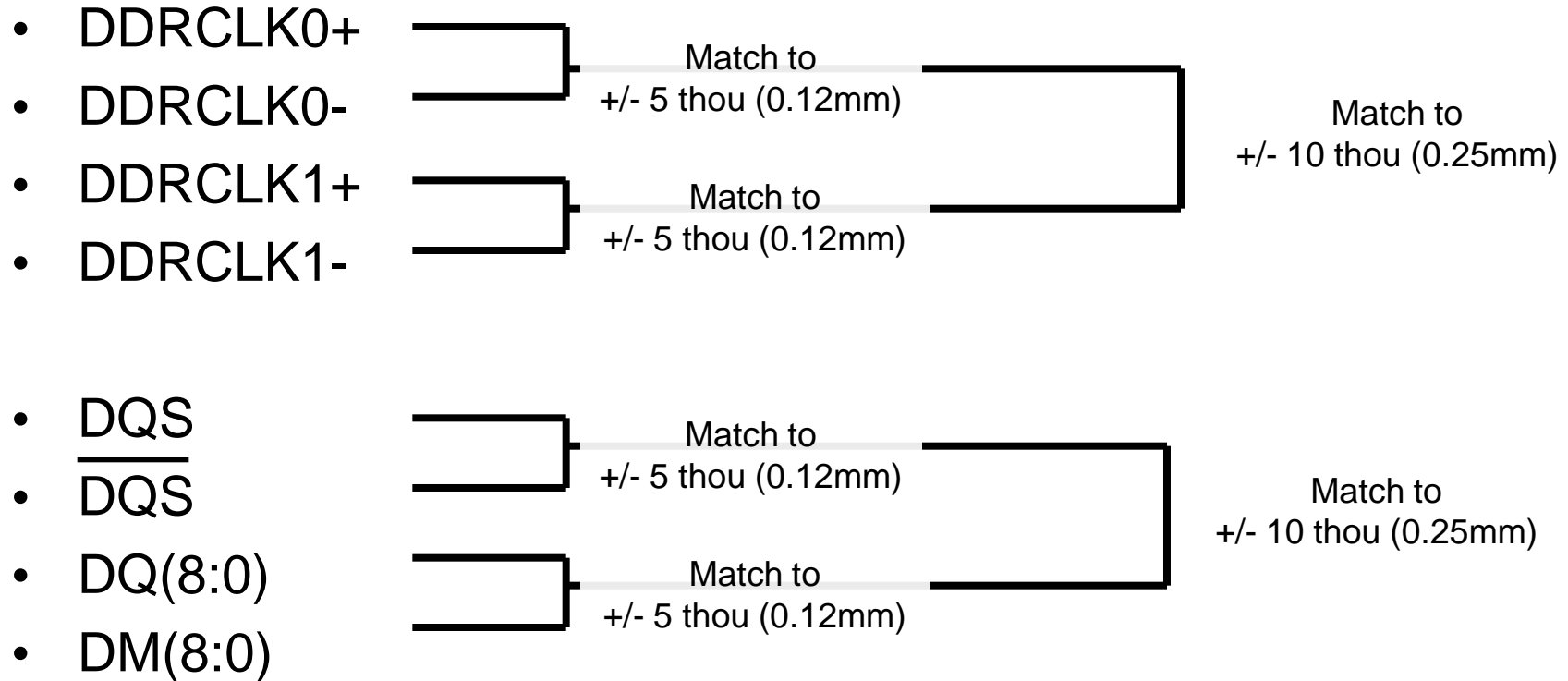
- Spacings
 - Data, Control & Clock - (unclassified) 25 thou \ 0.65 mm
 - Data – Data & Control - Control 7-10 thou \ 0.18 – 0.25 mm
- Max Skew
 - Across Byte lanes 500 thou \ 12.5 mm
 - Byte lane Data to strobe 20 thou \ 0.5 mm
 - Between differential Clock pairs 10 thou \ 0.25 mm
 - Between Clock pairs 25 thou \ 0.65 mm
- Layers
 - Clocks on a separate layer or adjacent to their signal groups
 - Critical signals routed on a layer adjacent to a reference plane

What is Skew?

- ‘A measure of the lack of symmetry’
 - In practical terms, the difference in time between the required and actual transit times of a number of synchronised signals
- Often more important than absolute signal timing or track length
 - If Signal Integrity is good

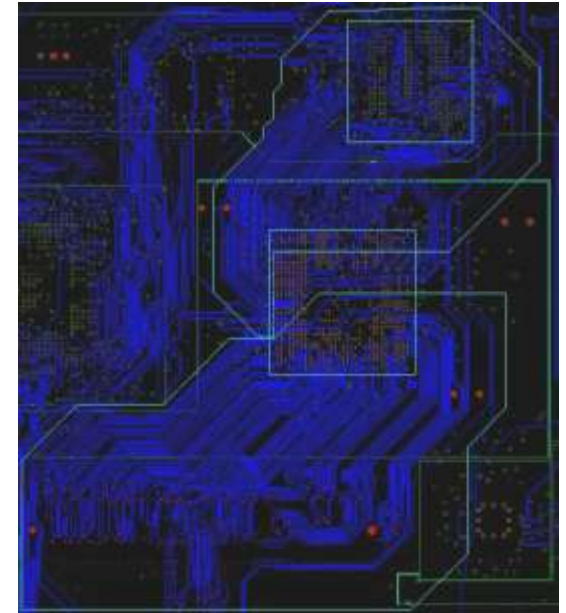


Clock group Skew Constraints - Example



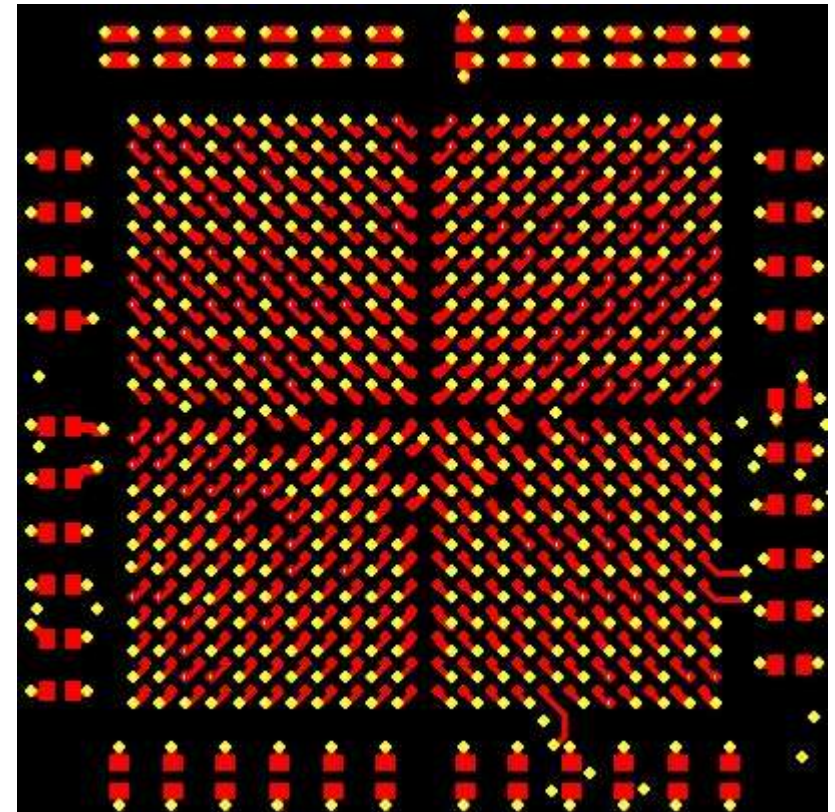
General Design Considerations

- Clocks to noisy signals or devices
 - Use Spacing Class to denote 'noisy' nets
- Plane Splits
 - Critical nets must be routed in relation to a contiguous reference plane
 - Consider adding Areas to denote split lines
- And Finally.....
- Verify your setup with your board fabricator
 - Layer Stack and Materials
 - Design Rules
 - Electrical and Manufacturing
 - Impedance profiles



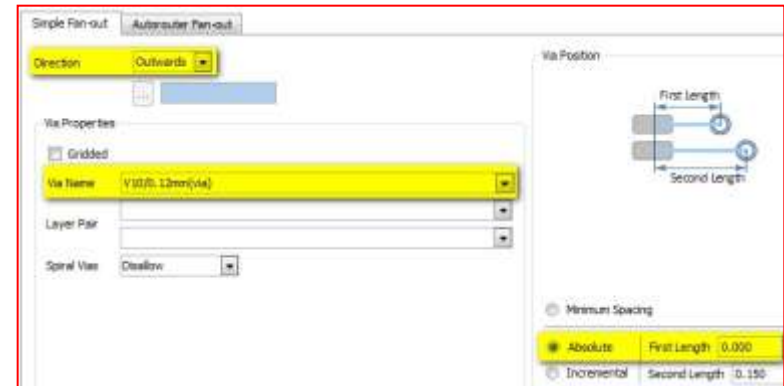
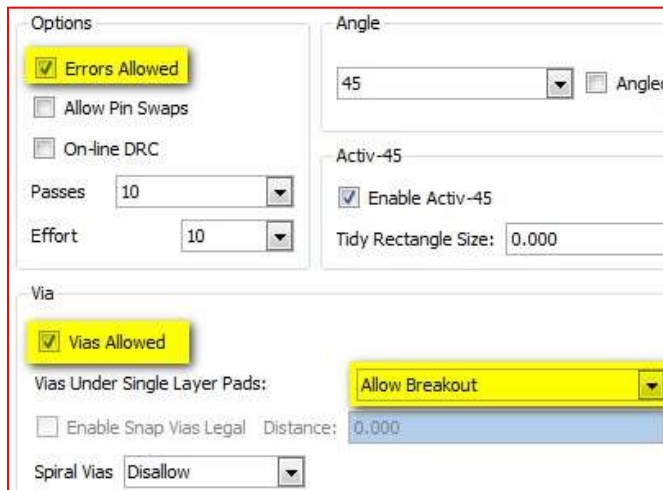
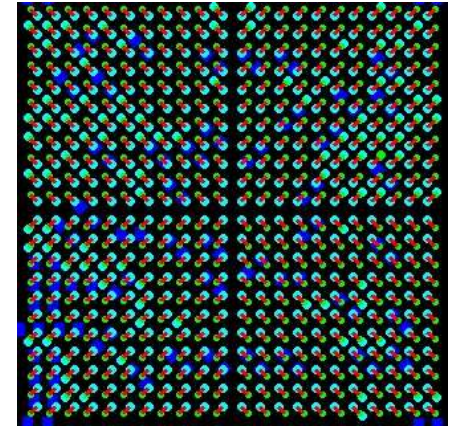
Implementation: Placement and Pre-Routing

- Pre-Placement
 - Minimum component spacing
 - Mirrored component arrays
- Terminators (if not ODT)
 - Position
 - Distance from Source
- Decoupling
 - Multi-rail devices
 - Managing Power Integrity
- Fanout
 - Geographic
 - Routing channels



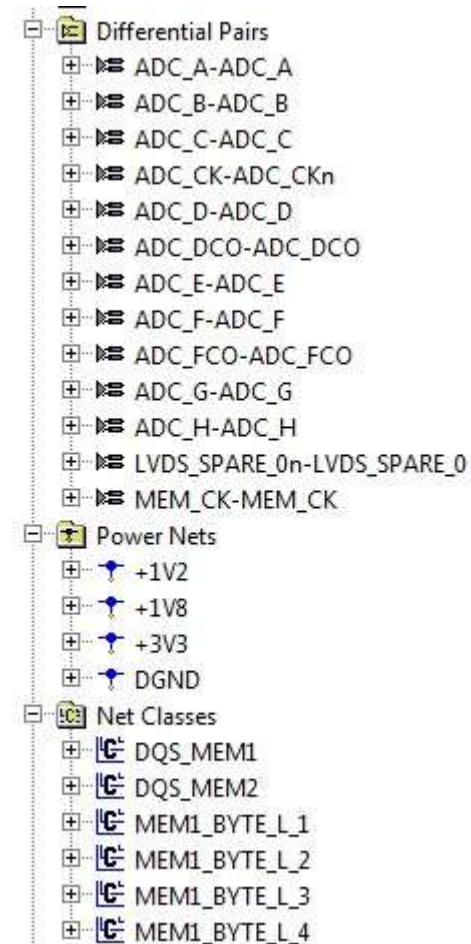
Fan-out Control

- Select Via type and Layer range
- Select Via location
 - Adjacent, angle
 - Via in Pad
 - Enable 'Allow Breakout' and check 'Absolute' spacing value



Setting up Bus and Group Structures

- Groups
 - Address
 - Data
 - Control
 - Clock
- Sub Groups
 - Byte Lanes
- Skew Groups
 - Clock-dependant sets
 - Bus items
 - Control
 - Clock
 - may be a differential pair



Impedance Controlled Routing

- Create Impedance Profiles
 - Single ended (Z0)
 - Differential (Zdiff)
- Assign to eNet, Bus, DiffPair, etc..
 - Manage only those nets with a specific requirement, not the entire board

Layer Stack Z0 Planning Zdiff Planning

Impedance Templates: Impedance Template 1 [Add...] [Delete]

Template Solver: [Solve Current] [Solve All]

	Type	Width (th)	Z0 (Ohm)	Velocity (th/ps)
All		10.0		
1 (Component)	Signal	12.0	50.90	6.53
4 (VDD)	Full Plane	35.0	50.12	6.05
6 (Inner 1)	Signal	6.0	48.20	5.56
8 (Inner 2)	Signal	6.0	48.20	5.56
10 (GND)	Full Plane	35.0	50.12	6.05
13 (Solder)	Signal	12.0	50.90	6.53

Busses

- ADD
- Adress_Bus
- DATA**
- DATA0

	Aggressor	Layer	Impedance Template
DATA	All	All	Impedance Template 1

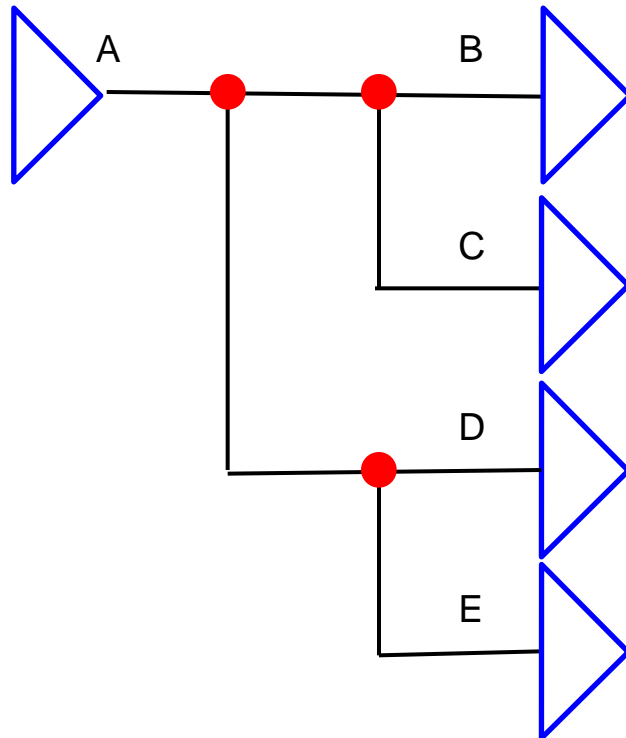
Impedance Templates: Impedance Template 1 [Add...] [Delete]

Template Solver: [Solve Current] [Solve All] Precision (

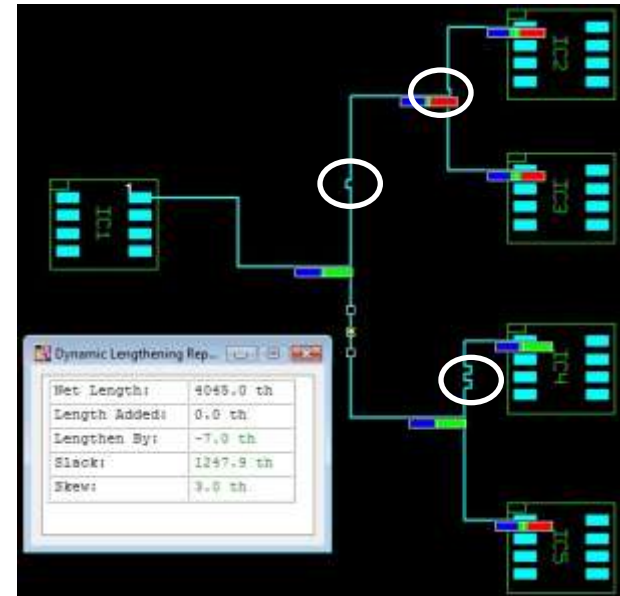
	Type	Width (th)	Spacing (th)	Z_diff (Ohm)	Z_odd (Ohm)	Z_even (Ohm)	Z_common (Ohm)	v_diff (th/ps)	v_odd (th/ps)	v_even (th/ps)	v_common (th/ps)
All			8.0	100.00							
1 (Component)	Signal	9.4			50.23	65.06	32.53	6.97	6.97	6.35	6.35
4 (VDD)	Full Plane	7.6			50.04	123.77	61.89	5.79	5.79	6.04	6.04
6 (Inner 1)	Signal	5.0	18.0		50.37	53.28	26.64	5.56	5.56	5.56	5.56
8 (Inner 2)	Signal	5.0	18.0		50.37	53.28	26.64	5.56	5.56	5.56	5.56
10 (GND)	Full Plane	7.6			50.04	123.77	61.89	5.79	5.79	6.04	6.04
13 (Solder)	Signal	9.4			50.23	65.06	32.53	6.97	6.97	6.35	6.35

Net Topology – Pin & Branch

- Match lengths for each branch
 - Within skew constraint



Objective:
 $A-B = A-C = A-D = A-E \pm 10 \text{ thou}$

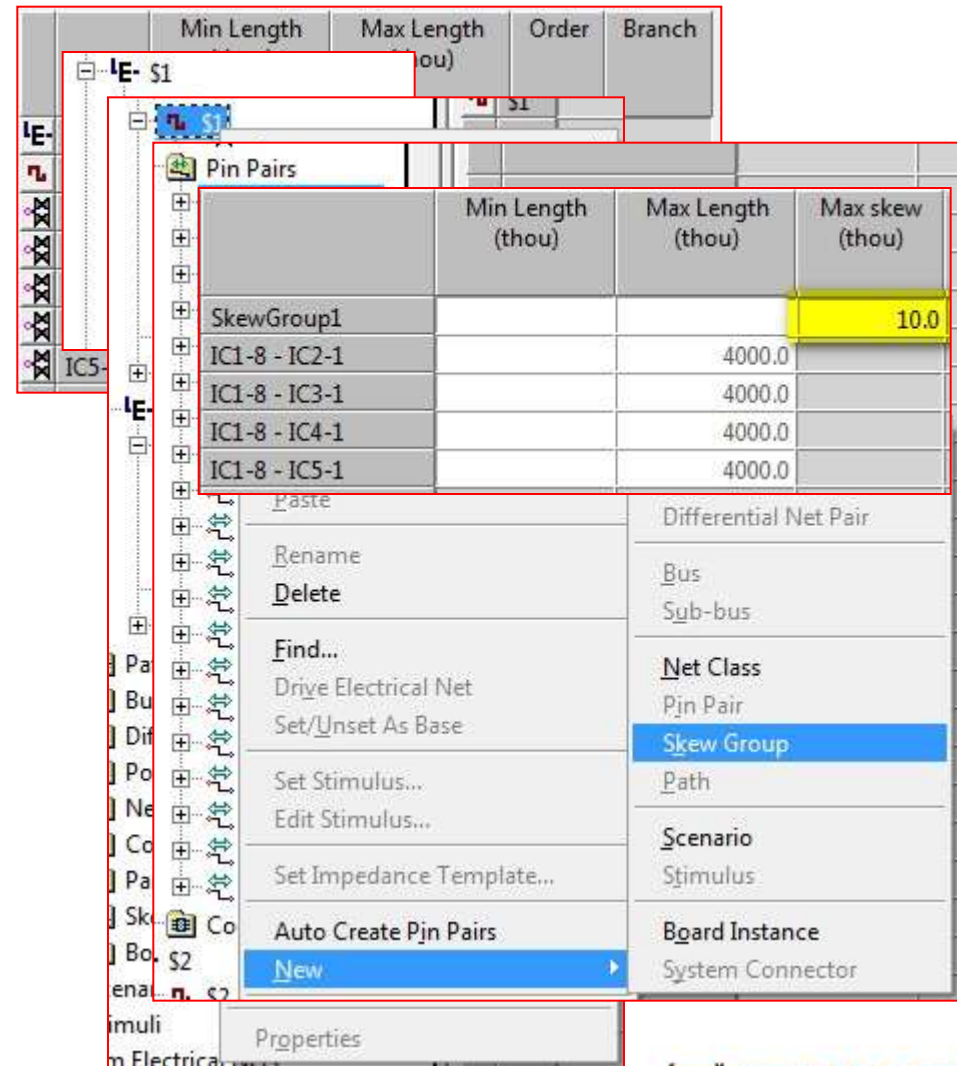


	Max skew (thou)	Min Length (thou)	Max Length (thou)	Max skew (thou)
SkewGroup1	10.0	1973.0	1976.0	3.0
\$1		846.0	2387.0	1541.0
IC1-8 - IC2-1		1976.0	1976.0	
IC1-8 - IC3-1		1974.0	1974.0	
IC1-8 - IC4-1		1973.0	1973.0	
IC1-8 - IC5-1		1975.0	1975.0	

Matched Length Pin Group - Example

- Setup Process

- Assign a Pin Order to the net on the common / Driver
- Select the Net and create / expand the Pin-Pairs
- Select the pin pairs and create a skew group
- Set the skew value

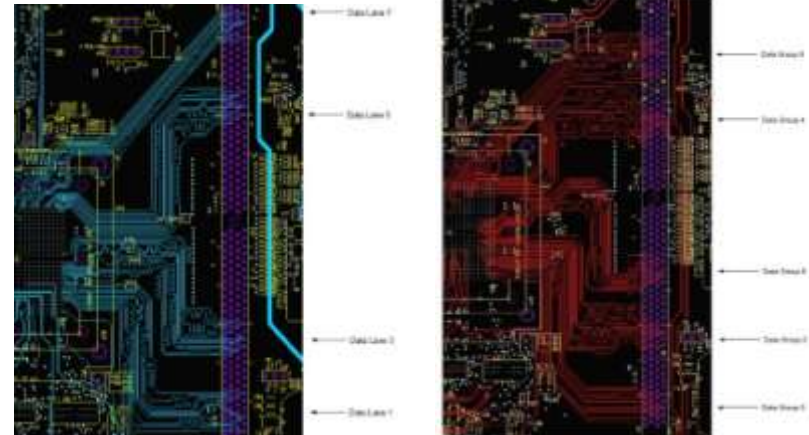
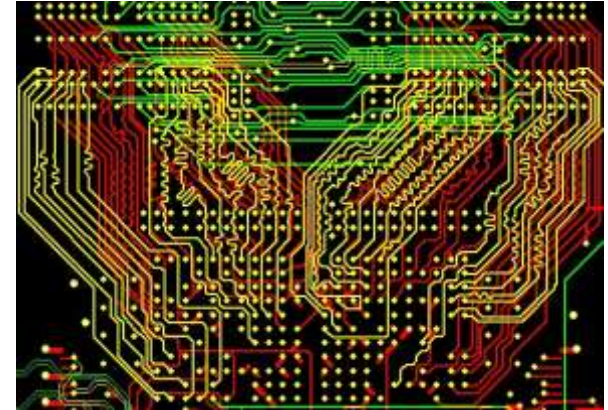


The screenshot shows a software interface with a table of Pin Pairs and a context menu. The table has columns for Min Length (thou), Max Length (thou), and Max skew (thou). The context menu is open over the table, showing options like Rename, Delete, Find..., Drive Electrical Net, Set/Unset As Base, Set Stimulus..., Edit Stimulus..., Set Impedance Template..., Auto Create Pin Pairs, and New. The 'New' option is highlighted, and a sub-menu is visible with 'Skew Group' selected.

Pin Pairs	Min Length (thou)	Max Length (thou)	Max skew (thou)
SkewGroup1			10.0
IC1-8 - IC2-1		4000.0	
IC1-8 - IC3-1		4000.0	
IC1-8 - IC4-1		4000.0	
IC1-8 - IC5-1		4000.0	

Split Bus / Group by Layer

- Meet spacing requirements
 - Design rules
 - Impedance matching
- Device dependant
 - Escape direction frequently organised by byte lane
- Provide sufficient room for length equalisation
 - Maximise space between byte lanes for improved noise immunity

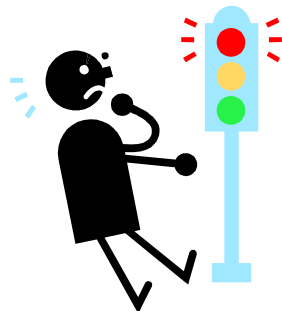


Clocks First?

- Determine optimal length
- Route and tune other nets to match the Clock
 - Data
 - Address
 - Control

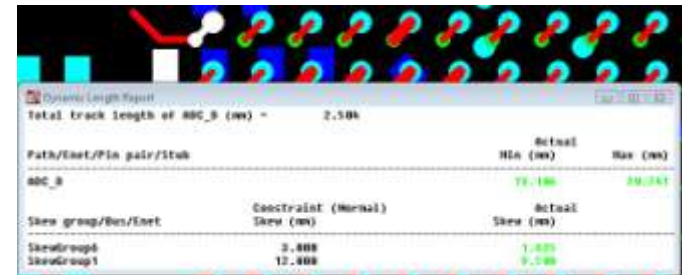
Clocks Last?

- Route 'other' nets first
 - Data
 - Address
 - Control
- Determine optimal length
- Tune all nets
- Route and Tune Clocks



Routing to Length

- Display Dynamic Length Report
- Use Constraint Indicators
 - Min / Max
 - Scale



Dynamic Length Report

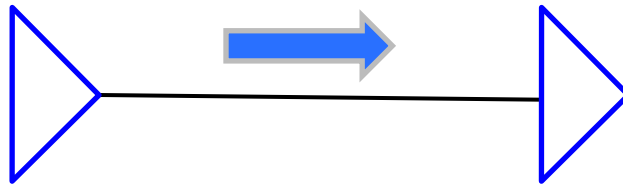
Total track length of ABC_B (mm) = 2.50k

Path/Net/Pin pair/Stub	Actual Min (mm)	Actual Max (mm)
ABC_B	19.19k	20.04k

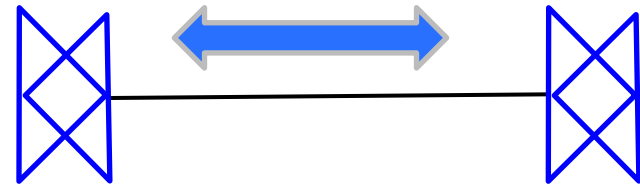
Skew group/Bus/Net	Constraint (Normal) Skew (mm)	Actual Skew (mm)
SkewGroup6	3.40k	1.80k
SkewGroup1	12.40k	9.50k

Length v. Delay Rules Routing

- Time / Delay based rules are far more complex than Length
 - Frequency dependant
 - Slower to calculate
 - More accurate



L = 100mm
IC1.td = 90ps (typical)

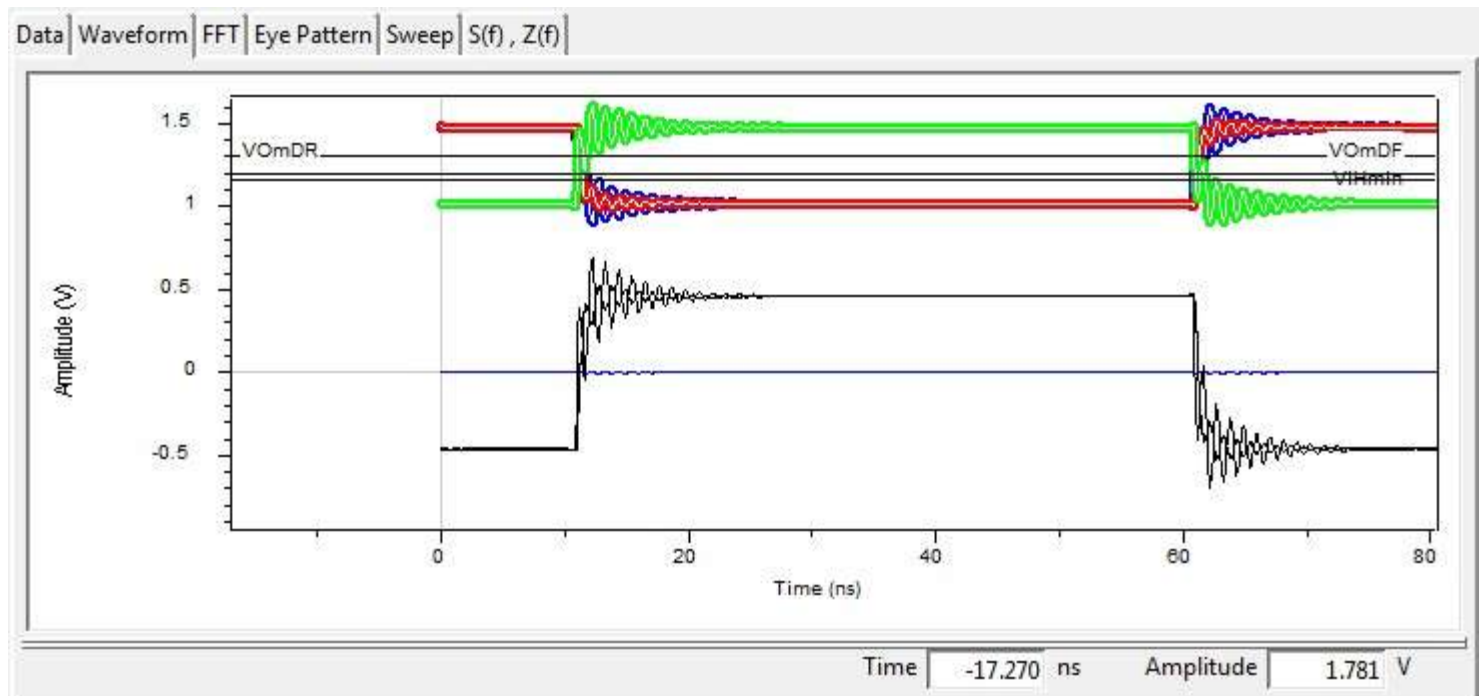


L = 100mm
IC1.td = 90ps
IC2.td = 80ps

IC1.tf = 110ps
IC2.tf = 75ps

Timing \ Delay Factors

- Switching speed of the device(s)
- Termination strategies
- Other factors



- Rules
- Constraints
- Crosstalk
- Manufacturing
- Signal Integrity
- Power Integrity

- Vendor Quote(s)'''

Freescale Semiconductor
Application Note

Document Number: AN2910
Rev. 2, 03/2007

Hardware and Layout Design Considerations for DDR2 SDRAM Memory Interfaces

by DSD Applications
Freescale Semiconductor, Inc.

The design guidelines presented in this document apply to products that leverage the DDR2 SDRAM IP core, and they are based on a compilation of internal platforms designed by Freescale Semiconductor, Inc. The purpose of these guidelines is to minimize board-related issues across multiple memory topologies while allowing maximum flexibility for the board designer.

Because numerous memory topologies and interface frequencies are possible on the DDR2 SDRAM interface, Freescale highly recommends that the system/board designer verify all design aspects (signal integrity, electrical timings, and so on) through simulation before PCB fabrication.

.....	2
.....	7
.....	7
.....	8
.....	8
.....	8
.....	9
.....	9
.....	12
.....	12
.....	13

© Freescale Semiconductor, Inc., 2005, 2007. All rights reserved.



Conclusion

- DDR2?
- Simple!
 - If you follow a systematic approach
 - If you use appropriate automation tools

